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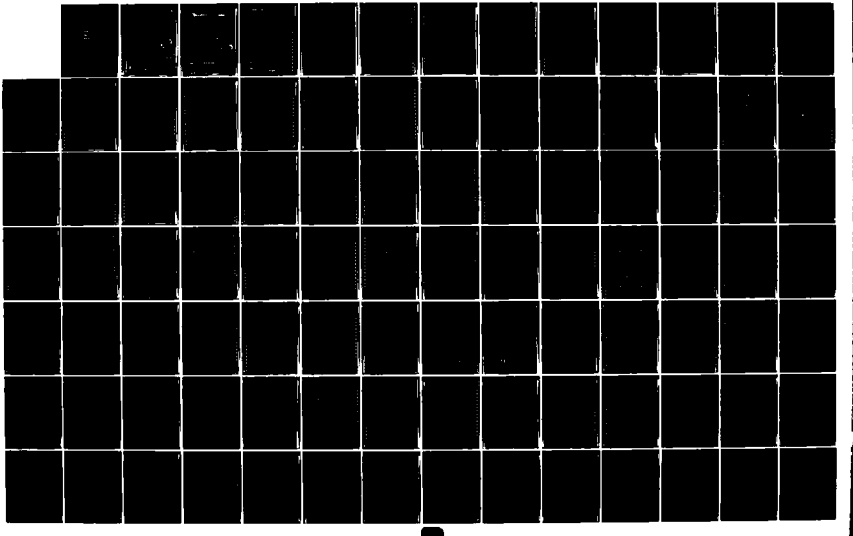

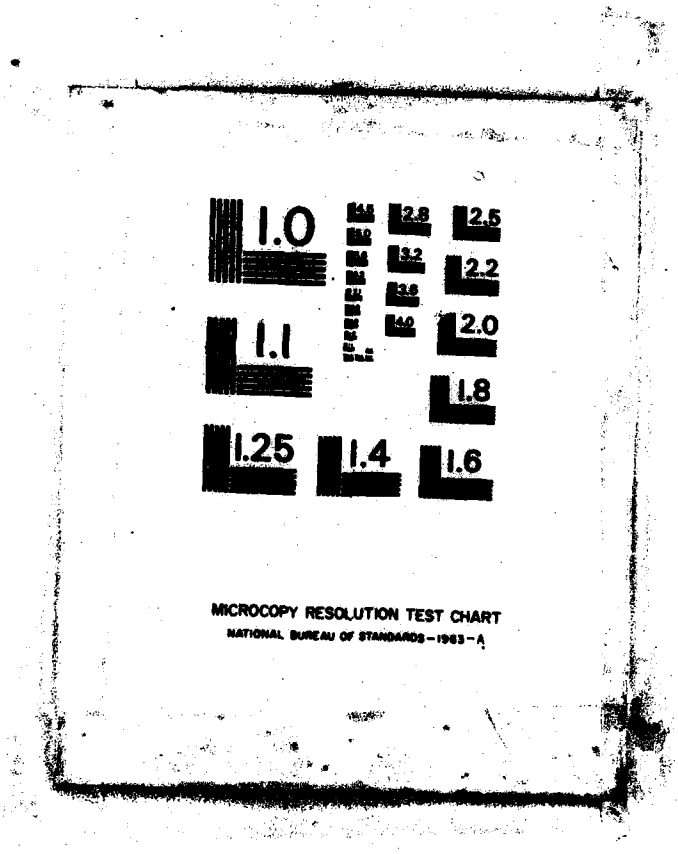
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FINAL REPORT

LOS SELECTIVE FADING AND AN/FRC-170(V) RADIO HYBRID COMPUTER SIMULATION

Contract No. DCA100-81-C-0016

SEPTEMBER 1982

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Prepared by

Engineering Computing Center

Martin Marietta Corporation
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AN/FRC-170(V) Radio	Equaliser	Bit Error Rates
LOS Channel	Microwave Fading Channel	Phase Lock Loops

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report documents results of the modeling, simulation and study of the dual diversity AN/FRC-170(V) radio and frequency selective fading microwave line of sight radio channel. Both hybrid computer and circuit technologies were used to develop a fast accurate and flexible simulation tool to investigate changes and proposed improvements to the design of the AN/FRC-170(V) radio.

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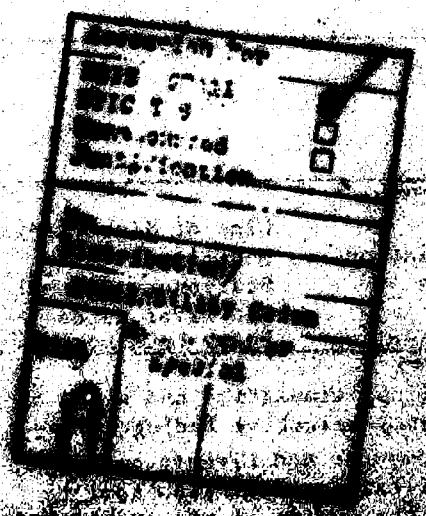
In addition to the simulation study, a remote hybrid computer terminal was provided to DCEC for interactive study of the modeled radio and channel.

Simulated performance of the radio for Rayleigh, line of sight two ray channels, and additive noise are included in the report.



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FOREWORD

This report documents the hybrid simulation, designed and maintained by Martin marietta Aerospace in Orlando, Florida, of the DCS AN/FRC-170(V) dual diversity radio. Areas of special interest to this report are those tasks outlined in statement of work R220-81-11 as part of contract number DCA100-81-C-0016. Those tasks include the modeling and implementation of an improved signal quality monitor, an improved diversity combiner, an adaptive threshold technique for carrier, clock and data recovery, enhancement and implementation of the existing baseband equalizer model, along with an IF slope equalizer. Other improvements addressed in this report which are specified in the statement of work are the internal time division multiplexing framing pattern, the CRT hardcopy of BER vs EB/NO, an indication of fade outage measured in percent time spent below threshold as defined in DCEC Technical Note 12-76, and reconfiguration of the simulation into modular form to allow for implementation of future product improvements.

A flexible and accurate computer simulation of the dual diversity line-of-sight DRAMA radio terminal and multipath fading channel has resulted from this simulation study. Mathematical models and hybrid computer simulations of the DRAMA radio systemwere designed by Martin Marietta's Engineering Center, Orlando, Florida, in support

of the Transmission Engineering Directorate, Transmission Systems Division of the Defense Communications Engineering Center, Reston, Virginia.

Provisions of this contract included the placement of a hybrid computer remote terminal at the Defense Communications Engineering Center. This terminal was used by the center's engineers to control the simulator, test the system under simulated channel effects, and extract system performance data.

CONTENTS

ILLUSTRATIONS

1.0 INTRODUCTION

This report discusses and documents a 18-month hybrid computer simulation study of the dual diversity AN/FRC-170(V) radio and line of sight (LOS) selective fading channel. The simulated LOS transmission system includes the transmit and receive circuits of the dual diversity radio and frequency selective LOS channel. The modular system design allows model enhancements to be integrated into the system model.

The present simulation has taken advantage of models, simulations and results of previous contracts DCA 100-77-C-0061 and DCA 100-79-C-0048, and includes enhancements outlined as tasks in statement of work R220-81-11 of this contract. These tasks will be briefly reviewed here and delineated in Chapter 2. Included in Chapter 2 are references to a more detailed technical discussion that is contained in the DRAMA radio model description of Chapter 3.

Tasks 1-5 included the following:

- Task 1 required the modeling and simulation of an improved dual diversity combiner.
- Task 2 specified the development and implementation of an improved signal quality monitor (ISQM).
- Task 3 specified an improved baseband equalizer and an IF adaptive equalizer to be integrated into the simulation.

- Task 4 required that the contractor provide and maintain for DCEC an accurate simulation of the AN/FRC-170(V) radio and frequency selective fading LOS radio channel, using the work performed under DCA contract DCA 100-79-C-0048 as a baseline system. Task 4 also required inclusion of a time division multiplexing (TDM) framing pattern into the aggregate bit stream, a CRT and hard copy plot of Bit Error Rate (BER) vs EB/NO, indication of fade outage measured in percent time spent below threshold and reconfiguration of the simulation into a modular form to allow for future upgrades.

- Task 5 includes the development of interactive displays and controls to be provided for the remote hybrid terminal user at DCEC.

Tasks 1 and 2 were primarily accomplished during Phase A and tasks 3, 4 and 5 were accomplished during Phase B of this contract.

Chapter 3 covers all technical aspects of the simulation of the AN/FRC-170(V) radio and frequency selective fading radio channel. Chapter 4 covers the model from the digital control point of view. An overview of the digital portion of the simulation is given and user options and commands are discussed in detail. Chapter 2 also makes references to those sections where new capabilities have been provided during this reporting period.

Chapter 5 documents customer runs and results which have typified use of the simulation during the last reporting period. Chapter 6 contains a summary of this report. Within the Appendices can be found a discussion of the Intel 2920 digital signal processor and its application to communications simulation. In addition, a complete set of all current analog computer diagrams is documented.

2.0 DISCUSSION OF CONTRACTUAL TASKS

This chapter discusses Tasks 1-5 as outlined in statement of work R220-81-11. In addition, further enhancements made to the simulation during this reporting period are discussed. References to Chapters 3 and 4 will be made for more detailed technical information.

2.1 Task 1 Discussion

Task 1 requires the modeling and simulation of an improved dual diversity combiner for the AN/FRC-170(V) radio. The combiner model has been implemented into the hybrid computer simulation. A choice of the Improved Signal Quality Monitor (ISQM) or Received Signal Level (RSL) diversity selection is available to the user, thus providing both the old and new diversity algorithms. The dual diversity combiner is discussed in more detail in section 3.16 and examples of its use are shown in section 4.

2.2 Task 2 Discussion

Task 2 specifies the development and implementation of an Improved Signal Quality Monitor (ISQM) simulation and implementation of this into the AN/FRC-170(V) hybrid computer simulation. The ISQM was based on a pseudo-error technique provided by the government. The model has been implemented into the hybrid computer simulation and is available as a user option. Several pseudo error counter options have been provided for the ISQM and a hysteris analysis multiple run averaging

option has also been made available. These options have all been used extensively by engineers at the Defense Communications Equipment Center, through the remote terminal link. A detailed discussion of the technical aspects of the ISQM can be found in section 3.15 and examples of the required remote user interaction in section 4.6.

2.3 Task 3 Discussion

Task 3 addresses the modification to be made to the existing baseband equalizer. An additional analog console was utilized for implementation of the improved baseband equalizer and special purpose hardware was built up to implement the delay lines required. A block diagram and discussion of the equalizer implementation are contained in section 3.10. In addition, an IF slope equalizer was designed and added to the hybrid computer simulation model. The slope equalizer placement is at the output of the IF amplifier.

The equalizer design compensates for (1) linear slope selective fading over the spectrum bandwidth, up to $\pm$ 14 dB magnitude at a maximum fade rate of 100 dB/sec, and (2) notch selective fades over the spectrum bandwidth, up to 14 dB of amplitude null at a maximum fade rate of 100 dB/sec. Section 3.7 contains a description of the hybrid simulation IF equalizer model and includes a block diagram. Task 3 was primarily accomplished during phase B of this contract.

2.4 Task 4 Discussion

Task 4 required that the contractor provide and maintain for DCEC an accurate simulation of the AN/FRC-170(V) radio and frequncy

selective fading radio channel, using the work performed under DCA contract number 100-79-C-0048 as a baseline system. The hybrid simulation has been made available to engineers at the Defense Communications Engineering Center, through the remote hybrid terminal link. In particular, Mr. Stanley Soonachan and Dr. Dave Smith have made extensive use of the simulation, resulting in many hundreds of hours of use over the contract period. Each day that the simulation was to be used, Martin Marietta Aerospace engineers went through a setup and verification procedure to ensure that the simulation met all accuracy requirements. They also have been available to assist in making runs and to provide technical assistance, as required.

Also required by Task 4 was the inclusion of a time division multiplexing (TDM) framing pattern into the aggregate bit stream. A discussion of the implementation and a flowchart is contained in section 3.2. In addition, a CRT and hard copy plot of Bit Error Rate (BER) vs EB/NO was required. A discussion of this user option and sample plots can be found in section 4.6.

Task 4 requirements included an indication of fade outage measured in percent time spent below threshold, as defined in DCEC technical note 12-76. A discussion and block diagram of the fade outage monitor routine is included in section 3.17. The preceeding Task 4 enhancements were accomplished during Phase B of this contract.

Reconfiguration of the simulation system into modular form to allow for future upgrades was also required. The simulation has been setup in a modular form to accommodate any future changes.

A technical description of each module can be found in Chapter 3. The simulation was also reconfigured to allow for upgrades, such as a new 5 watt linear amplifier to replace the present TWT, a tunable transmit and receive frequency and an RF jamming/RFI indicator.

2.5 Task 5 Discussion

Task 5 includes the development of all interactive dispalys and controls to be provided for the remote hybrid terminal user at DCEC. These have included the following:

- Display of all available program options
- Summary display of simulation configuration showing program options and parameter choices selected by the simulation operator
- Spectrum Analyzer Display of power density spectrum at baseband, IF and RF (pre- and post-amplification filtering)
- Tabular listing of experiment Bit Error Rate for non- and dual diversity
- Baseband eye patterns for cophasal and quadrature QPR modem branches
- Logarithmic fading channel envelope displays (analog) vs time
- Diversity switch status (on-line indications for channel "A" or channel "B")
- Channel Distribution Function
- Other displays as deemed necessary to the effective and efficient operation of the simulation.

The last requirement of this task was the provision for a hybrid computer remote terminal to be made available at DCEC for engineering use in verification and analysis of the simulated LOS

transmission system. A description of these interactive displays and controls can be found in Chapter 4.

2.6 Additional Enhancements

Other improvements which have been incorporated into the simulation include enhancements to the channel model. These enhancements were implemented during Phase B of this contract. The ability to specify individual EB/NO for each receiver channel is now available. The option to specify individual power profiles for each channel has been provided. A more organized user interactive input routine for channel parameter definition was programmed. In addition, channel model cut off frequency limits have been extended to 0.<Fco<=1. A technical description of the enhanced channel model can be found in section 3.5. User options are demonstrated in section 4.5.6.3 and 4.5.6.4.

The inclusion of the adaptive threshold technique for carrier, clock, and data recovery was accomplished during this contract period. This modification has been fully checked out and is now a permanent part of the model. A detailed discussion of its final implementation is included in section 3.9.

An area of continuing research and development during this contract period has been the application of the Intel 2920 digital signal processing chip to the modeling of high order filters in the AN/FRC-170(V) simulation. A fifth order receive baseband filter has been implemented on the 2920 chip and frequency responses made. Appendix A documents the progress made to date.

Other enhancements include increasing the AGC bandwidth limits to .001 Hz <= Fco <= 10 Hz, rescaling the baseband and carrier phase lock loop signal levels to increase system accuracy and repeatability, and provision of a new pot verification and setting routine improve simulation verification and reliability.

3.0 AN/FRC-170(V) RADIO AND LOS CHANNEL SIMULATION

This section describes the current simulated model of the AN/FRC-170(V) radio and line of sight channel. It includes additions and circuit modifications needed to maintain an accurate, modular, and flexible waveform simulation of the LOS radio and channel characteristics. References to this chapter are made from Chapter 2, in order to pinpoint areas which describe work completed under DCA Contract, DCA100-81-C-0016. Figure 3-1 is a functional flow diagram of the current system, including the transmitter, channel model, and receiver.

The major systems of this LOS transmission system model are the dual diversity radio, dual LOS frequency selective fading channels, performance monitors, diversity combiner, and an interactive user display and control program that allows off-site operation from DCEC, Reston, Virginia.

3.1 Drama Radio Model

The simulated model of the dual diversity AN/FRC-170(V) radio includes all of the important functional characteristics unique to the actual radio. These include the capability to simulate level I quadrature phase shift keyed (QPSK) transmission and level II

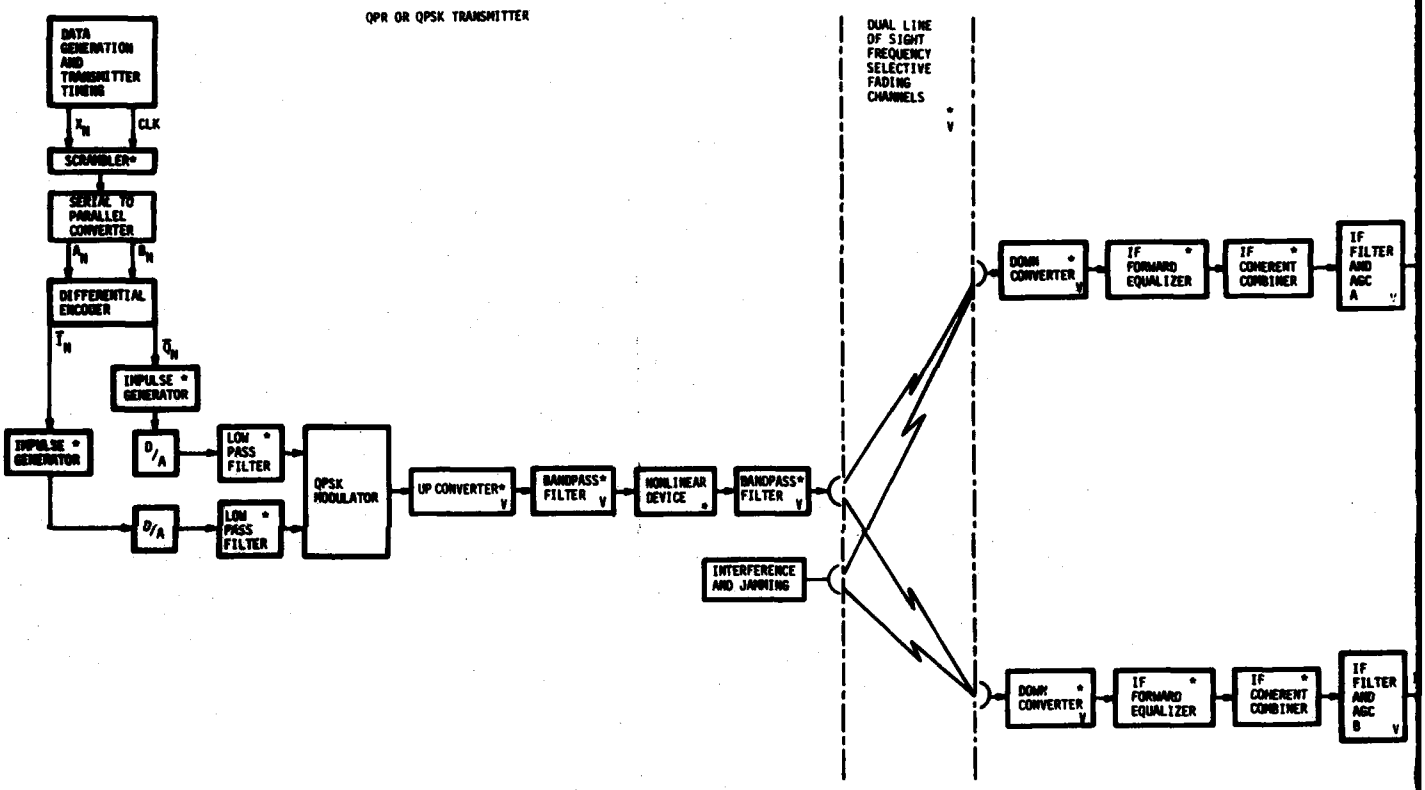
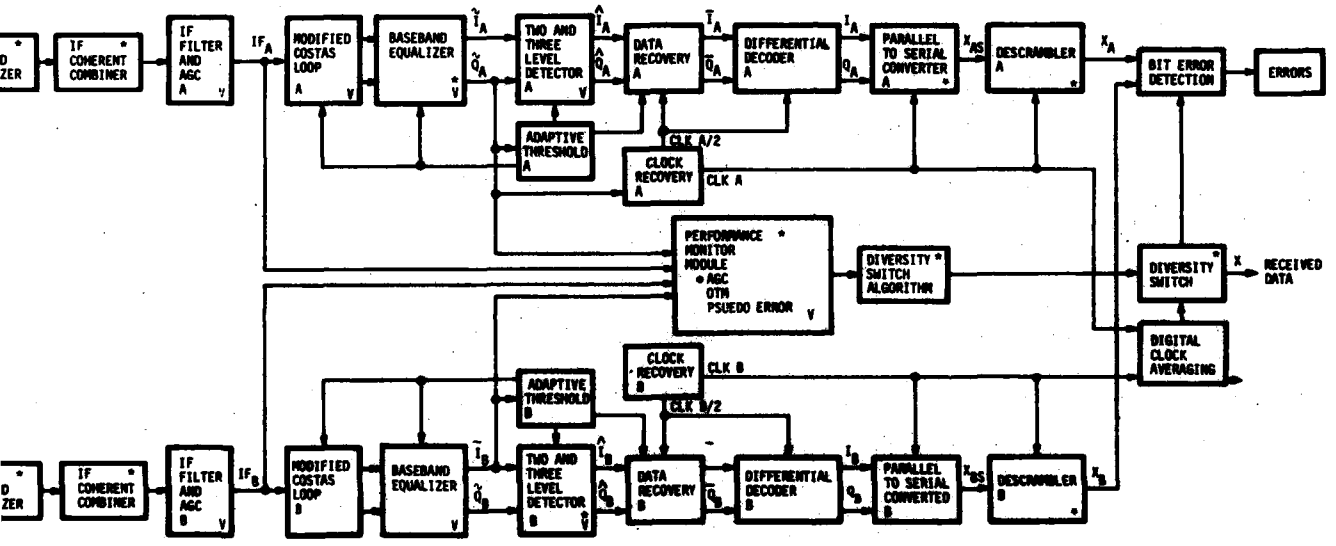


Figure 3-1. AN/FRC-170(V) LOS Simulation Model

QPR OR QPSK RECEIVERS



* - OPTIONAL MODULE
V - VARIABLE MODULE

quadrature partial response (QPR). Selection of one or the other modulation scheme can be accomplished almost instantaneously by the simulation user. Major modules of the dual diversity AN/FRC-170(V) radio simulation are bit stream generation and processing, QPR/QPSK modulator, partial response filter, transmitter signal processing, channel model, IF equalizer, IF filter and AGC, modified Costas' loop demodulator, baseband equalizer, bit timing recovery, data regeneration diversity combiner and signal quality monitor. The models and simulation of these modules are discussed in the subsequent sections.

The hybrid computer simulation of the AN/FRC-170(V) radio provides an interactive scale model which can be configured and changed programatically by the simulation user to evaluate the resulting performance of product improvements and design changes for anticipated transmission channels. This simulation has been implemented by frequency scaling hybrid computer models of the prototype modem circuits and implementing these models with analog, parallel logic, and digital computing elements. The resulting computer simulation is more than 100 times faster than comparable waveform digital simulations. Two time scales are selectable in the simulator to provide a capability of simulating tap delays in the range of .025 to 2.5 data bits. The necessity of two time scales is a result of limited bandwidth of the digital delay device used in the channel model simulation. Normal time scale is unity (1) providing tap delays of .25 to 2.5 data bits and one-tenth (1/10) providing tap delays of .025 to .25 data bits. With the normal time scale selected a scale factor of 1/26,112 is used

to scale actual radio frequencies down to values that fit within the hybrid computer bandwidth. In the normal time scale mode real IF, bit stream and baseband frequencies of 70 MHz, 20.112 MHS and 13.065 MHS are simulated at frequencies of 2.0[illegible] KHz, 1 KHz and 300 Hz respectively.

3.2 Bit Stream Generation and Processing

The bit stream generation and processing module for the AN/PRC-170(V) radio is the same for both level I (QPSK) and level II (QPR) modes of transmission. This module includes the generation of a random data source with an optional [illegible] framing pattern insertion, a 20 bit self synchronizing scrambler, a serial to parallel converter and a differential encoder. [illegible] flow diagram of the integration of these circuits is shown [illegible].

The random portion of [illegible] the actual data to be transmitted is generated digitally by a pseudo random bit generator. [illegible] is desired, it is provided as an option. This option is [illegible] of the TDM framing flow chart in Figure 3-[illegible].

[illegible]

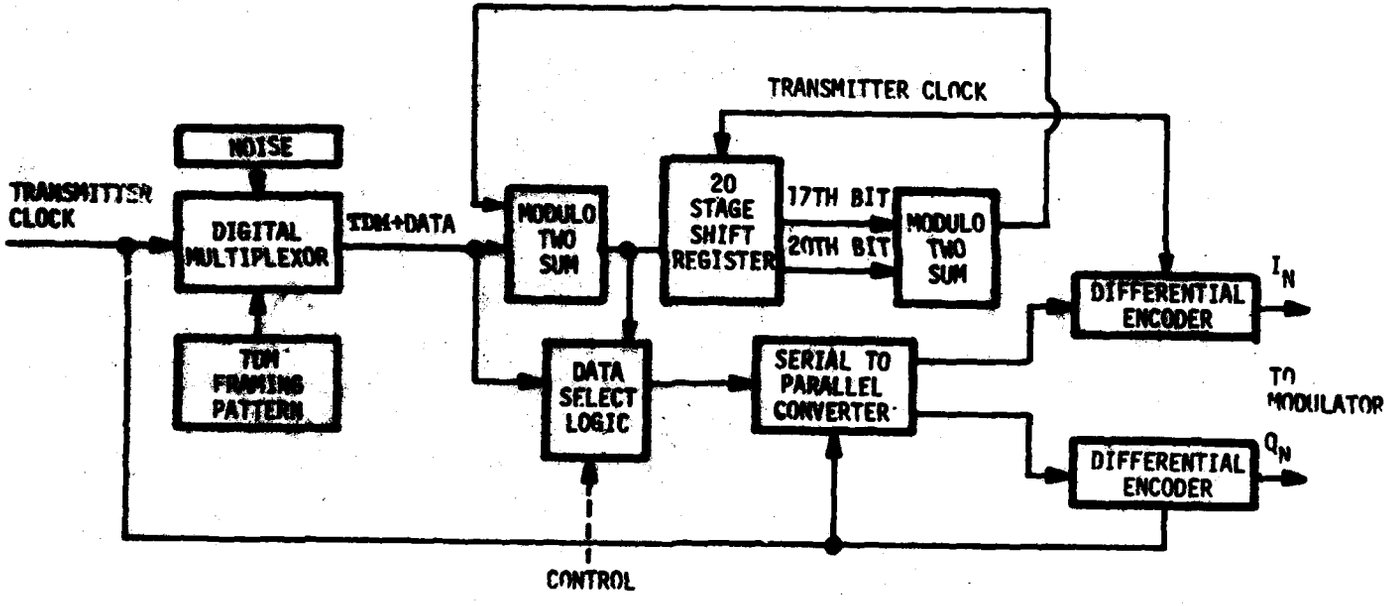


Figure 3-2. Data Generation and Processing

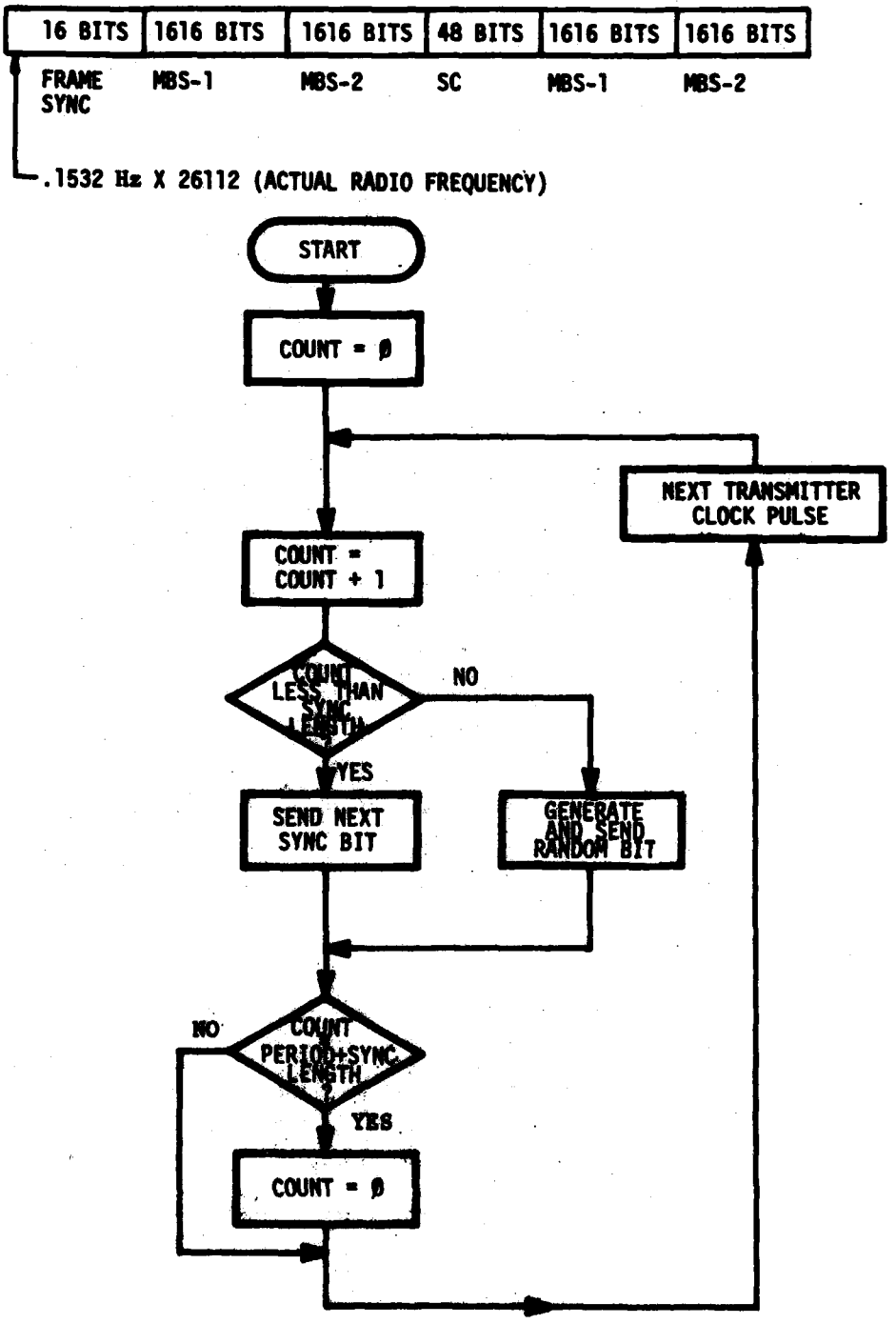


Figure 3-3. Bit Stream Generation

A self-synchronizing scrambler with 20 stages was modeled to ensure a random modulating bit stream. This circuit, which elimnates long series of ones and zeroes from occurring in the modulating bit stream, has been provided as an option. The randomness guaranteed by implementing the scrambler results in a better spectral component of the bit rate clock and provides a better likelyhood of clock recovery as a result of additional data transistions.

A model of the scrambler used in the AN/FRC-170(V) radio was obtained by modulo 2 summing the serial data stream with the modulo 2 sum of bits 17 and 20 from a 20 stage shift register. The 20 stage shift register was mechanized by ganging 5 four bit shift registers on the analog computer.

The serial to parallel converter was mechanized by retiming the scrambler output with the symbol clock (one-half the data rate). Symbol timing was used to clock the I and Q data with a one-half symbol delay with respect to one another. The delay between I and Q basebands improves resolution of the two-phase ambiguity states at the receivers.

Each of these parallel bit streams was input to differential encoders which resolve any polarity inversion at the demodulator. These encoders are modeled as a modulo sum (exclusive "OR"). This circuit does a logical multiply of the feedback and data. Outputs from the two encoders provide the inputs to the modulation circuit.

Except for data generation which consists of a digital random bit generator with a TDM framing pattern insertion option, the

entire data generation and processing module was simulated using the parellel logic capability of the analog computer. Modulo 2 sums and differential encoders were programmed using a combination of gates and flip/flop delays. The scrambler uses five 4-stage shift registers in series to provide the 20-bit delay. Serial-to-parallel conversion was simulated by using flip/flops enabled by inverted symbol clocks to provide a one-half symbol delay between one symbol bit stream and the other.

3.3 QPR/QPSK Modulator

The simulated AN/FRC-170(V) radio modulator section includes impulse generators for QPR transmission, digital-to-analog switches, transmit baseband filters, inphase and quadrature multipliers, and a crystal controlled reference oscillator. Input to the modulator module is from the I and Q differential encoders. Figure 3-4 is a functional flow block diagram of the major circuits for the modulator simulation. When QPR modulation is selected by the user, the I and Q modulation signals are generated by using the encoded I and Q return to zero logic to drive impulse generators. Each impulse stream becomes the driving function for one of the Class I partial response transmit filters, which provide the inputs to the inphase and quadrature balanced modulators. If QPSK modulation is selected, a path is provided directly from the encoded I and Q non return to zero (NRZ) data to the inphase and quadrature balanced modulators. The I and Q modulators outputs are summed to generate either QPR or QPSK signaling.

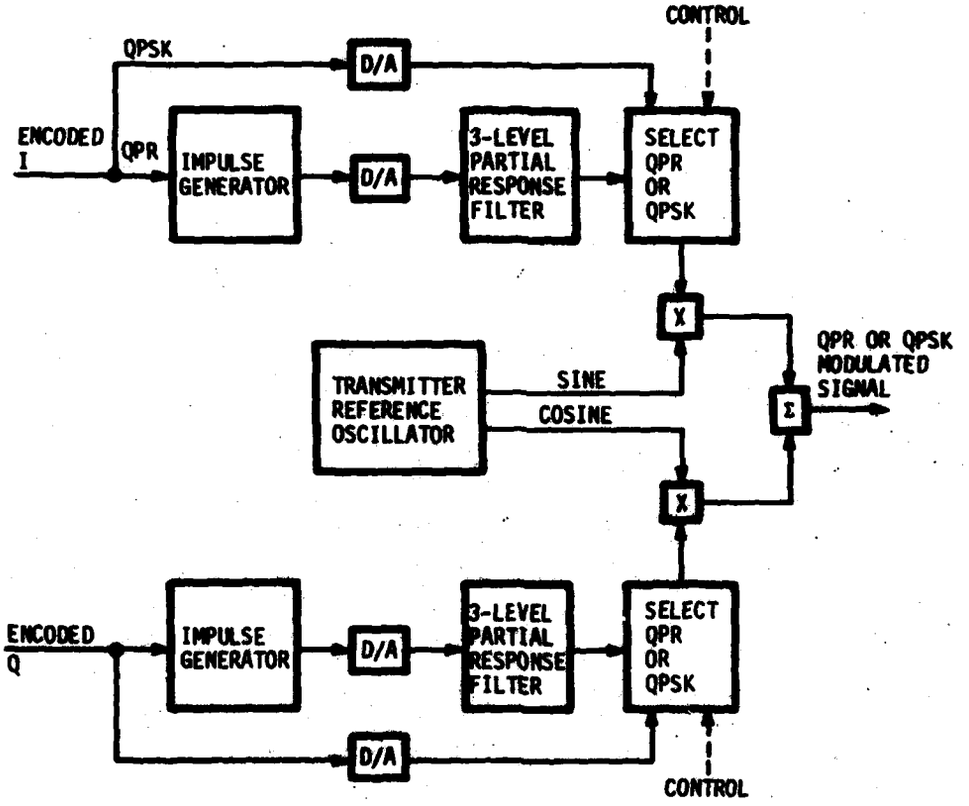


Figure 3-4. QPR/QPSK Modulator

The Class I partial response filters provide a controlled amount of intersymbol interference. Combined with the receiver baseband filters they approximate a cosine response that produces a three level signal at the receiver baseband output. In the simulation the transmit baseband filters are bypassed for QPSK.

Simulation models of the modulator circuits were programmed using both logical and analog computer techniques. Programs developed for the modulation functions and all other subsystems of the AN/FRC-170(V) radio are under the control of the digital computer segment of the hybrid computer. This approach makes parameter and configuration changes, set-up procedures and data acquisition very fast, and also provides needed documentation for every simulation test.

Encoded I and Q digital baseband signals are input to impulse generators if in a QPR mode, and to the quadrature multipliers if in a QPSK mode. The impulse generators were mechanized using monostable elements (one shots) of the parallel logic on the analog computer. These devices have an adjustable pulsewidth which was set to provide the desired impulse response from the partial response filters. The QPR or QPSK digital NRZ modulating signals were A to D converted using electronic digital-to-analog switches that generated plus and minus analog dc levels corresponding to the +1 and -1 logic.

If QPR was selected, these signals drove the I and Q transmit half of the partial response filters. When QPSK was selected, the digital computer sent control signals to the analog computer, which gated the encoded baseband signals directly to electronic switches and bypassed the partial response filters.

The processed baseband signals were input to four quadrant analog multipliers that multiplied the I and Q baseband with sine and cosine signals from the reference oscillator. The summation of these two multipliers resulted in either QPR or QPSK signaling, as determined by the simulation configuration selected by the user. A crystal controlled reference oscillator for this modulator section was programmed using two analog integrators with feedback to stabilize the amplitude and a crystal controlled digital clock to maintain a fixed frequency.

3.4 Partial Response Filter Model and Simulation

The transmit partial response filters were programmed from the transfer function:

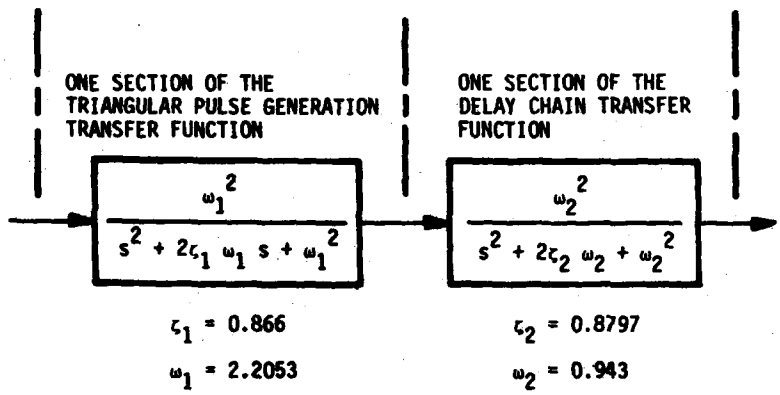
$$H(s) = \frac{3.25104}{s^4 + 4.3966s^2 + 9.28835s^2 + 8.105s + 3.25104}$$

Analog computer techniques for transfer function simulation were used to model these filters.

The partial response filters were designed to fit the frequency and the impulse response of a Class I, partial response filter. This approach ensured the desired intersymbol interference with adjacent pulses and prevented undesired intersymbol interference with other pulses.

The complete filter was mechanized as two identical fourth order stages, as shown in Figure 3-5. The first half is in the transmitter and the other half is in the receiver. The filter design was derived from a method based on the piecewise linear approximation to

the impulse response curve. This system model was designed by allotting fourth order transfer functions to the triangular pulse generator and the delay chain, each formed as the square of a second order transfer function. Thus the identical transmitter and receiver filters are formed from second order parts of the triangular pulse generator and delay chain.



WHERE s IS SCALED TO THE FILTER CUTOFF FREQUENCY

Figure 3-5. Partial Response Filter, Transmitter, and Receiver Filter Transfer Functions

The triangular pulse generator impulse transfer function is given by

$$T(s) = \frac{T}{2}\left[\frac{1 - e^{-s\frac{T}{2}}}{s}\right]^2 \simeq \left[\frac{\omega^2}{s^2 + 2\zeta\omega s + \omega^2}\right]^2$$

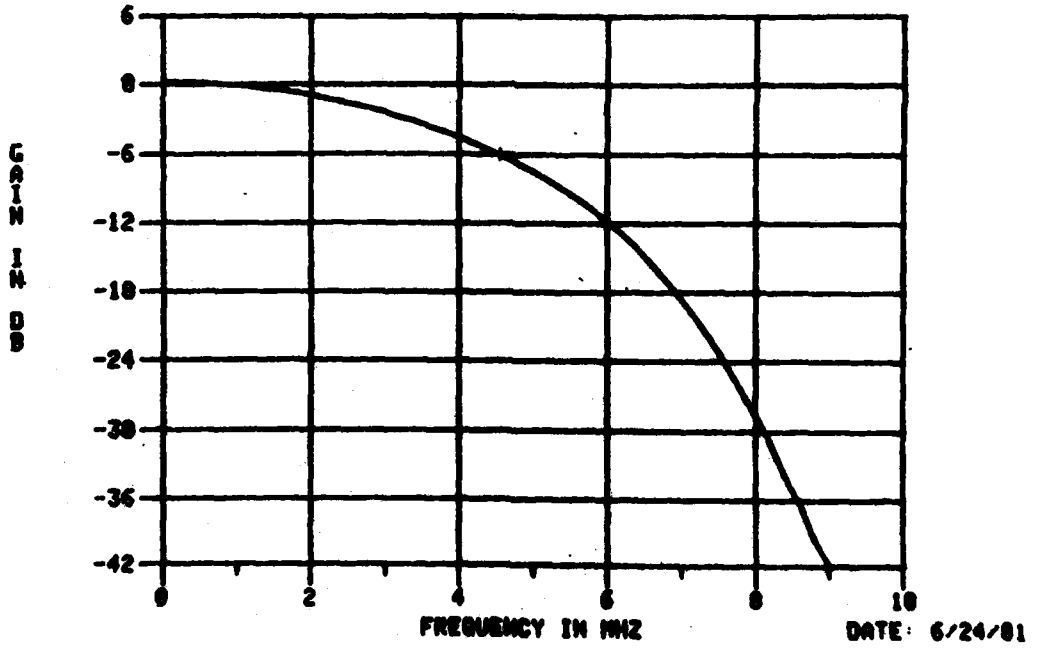
and its approximation was formed by equating the first few terms of the Taylor series for each.

The mechanized filter was tuned to give the desired impulse response. It has a bandwidth of three symbol pulsewidths and is essentially symmetrical about the peak. The filter has minimum inter-symbol interference at the third and fourth symbol pulse times.

The baseband filters currently being used are the same as those used in a previous QPR transmission model. A new set of partial response baseband filters using elliptical functions have been mechanized and tested that duplicate the response of those in the actual modem. The baseband transmit filters are modeled on the analog computers and the receive baseband filters are implementated utilizing Intel 2920 digital signal processing chips. These elliptical filters provide responses nearer to the actual AN/FRC-170(V) filters. Transfer functions of the transmitter elliptical baseband filters are given below.

$$H(S) = A \frac{a_o \omega_c}{S + a_o \omega_c} \prod_{i=1}^{3} \frac{S^2 + \Omega_i^2}{S^2 + 2a_i S\omega_c + (a_i^2 + b_i^2)\omega_c^2}$$

This filter is a 7th order elliptical lowpass filter whose parameters determine the bandwidth and attenuation characteristics. The analog simulated response using the following parameters is shown in Figure 3-6.



Filter parameters are:

Ω_1 = 1.4936

Ω_2 = 1.7741

Ω_3 = 2.9970

a_o = .6746

a_1 = .5279

b_1 = .6183

a_2 = .2741

b_2 = .9588

a_3 = .0793

b_3 = 1.0826

W_c = 1688 x 26,112 (ACTUAL RADIO FREQUENCY)

and 1688 *SIMULATED FREQUENCY*

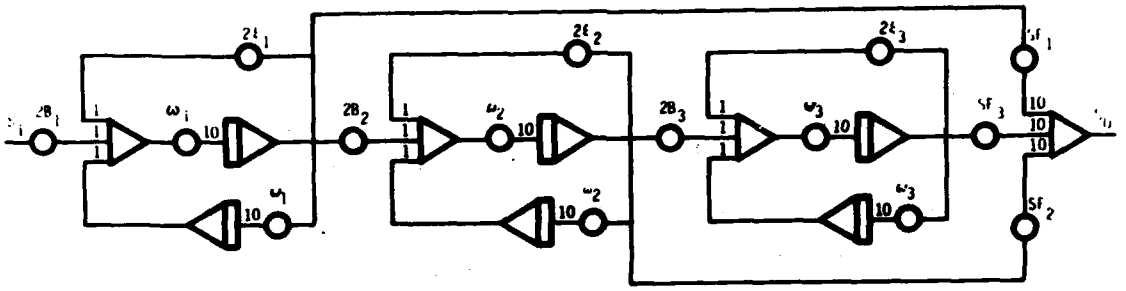
Figure 3-6. Simulated Response of the 7th Order Transmit Baseband Filter

3.5 Transmitter Signal Processing

A typical transmission section was modeled for the AN/FRC-170(V) radio. This configuration includes two transmitter bandpass filters for spectral limiting and a TWT power amplifier. All of these devices are modeled on the analog computer and can be configured by the simulation user. This RF portion of the transmission was simulated without the up and down conversion to RF frequencies; thus, the simulation was at IF frequency.

Optional spectral control bandpass filters and an optional nonlinear amplifier were simulated for the transmission module. These bandpass filters were programmed to permit the selection of either Butterworth, Bessel, or Chebychev characteristics for two, four, or six poles. A stagger-tuned simulation approach was taken, where the parameters for each stage were calculated and set by the digital computer, based on parameter inputs by the user for center frequency, ripple and bandwidth. The digital computer then calculates and sets the parameters of each stagger-tuned section to produce the desired overall frequency response of the filter.

Referring to Figure 3-7 the filter parameters β, ϵ, and ω of each stage represent the gain bandwidth product, bandwidth, and center frequency, respectively. SF_1, SF_2, and SF_3 are the scale factors that adjust the overall gain of the filter to ensure unity gain and select the order of the filter.



SIMULATES SECOND, FOURTH, OR SIXTH ORDER
CHEBYSHEV, BUTTERWORTH, OR BESSEL BANDPASS FILTER.

Figure 3-7. Bandpass Filter Simulation

The nonlinear device subsystem simulates the AM/AM and AM/PM characteristics of the AN/FRC-170(V) radio TWT.[1] The TWT simulation is shown in Figure 3-8. The card programed function generators have been replaced by a Multi-Function Table Processor (MFTP). Both the AM/AM and AM/PM characteristics of the DRAMA TWT are generated by the MFTP.

The MFTP is a high speed special purpose digital device designed to perform the operations of table lookup and linear interpolation in a manner to generate functions of one to four variables from preloaded data tables.

The modulated carrier is input to an envelope detector, which determines the time-varying amplitude of the carrier by diode-detecting the signal magnitude and filtering out the carrier frequency.

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(1) Thomas, C. M., Alexander, J. E., and Rahneberg, E. W., "A New Generation of Digital Microwave Radios for U.S. Military Telephone Networks," IEEE Transactions on Communications, Vol. Com-27, No. 12, December 1979.

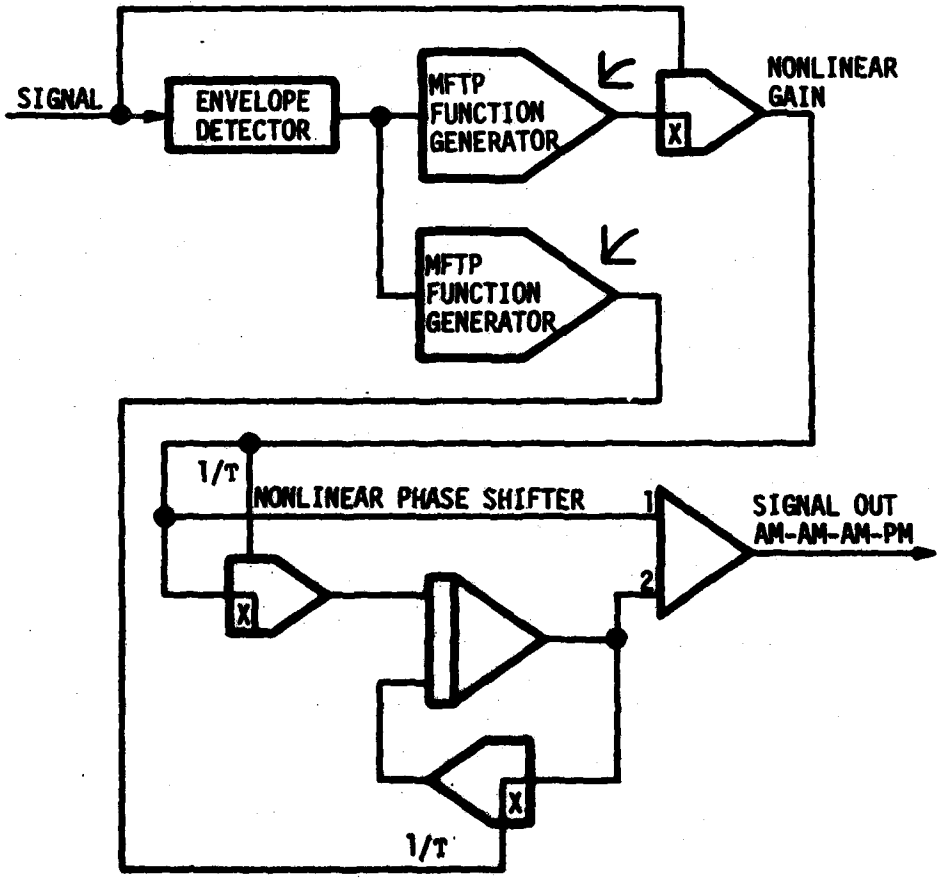

Figure 3-8. Nonlinear Device Implementation

This amplitude output drives the two functions in the MFTP which are loaded with the AM/AM and AM/PM characteristics of the nonlinear device. The output of the AM/PM function determines the time constants for an analog computer programmed phase shifter that shifts the modulated carrier by the corresponding gain. Graphs of AM/AM and AM/PM characteristics for the TWT are shown in Figures 3-9 and 3-10.

3.6 LOS Channel Model

The LOS simulator is made up of three elements: a delay line module, a digital filter module, and a multiplier-summer module. The simulation model allows the user to change the tap gains, tap delay spacing, and signal-to-noise ratio. Figure3-11 provides an overall block diagram of the channel model.

The delay line module is a special purpose device integrated into the hybrid computer system. It consists of charge-coupled device (CCD) integrated circuits (256 samples/tap), interconnection and tap output filtering circuits, clocking circuits, and a power supply. A frequency synthesizer, remotely controlled from the digital computer is used to provide the clock signal for the delay line. The clock frequency is chosen to provide a user specified delay between the taps. For example, a 2688 Hz signal and a clock frequency of 512 KHz yields a delay of 500 μs per tap (0.5 bits) and ~200 samples per cycle. The clock frequency can be changed to give an intertap spacing of between 0.25 and 2.5 bits at nominal time scale and .025 and .25 bits at .1 time scale. Each tap output is

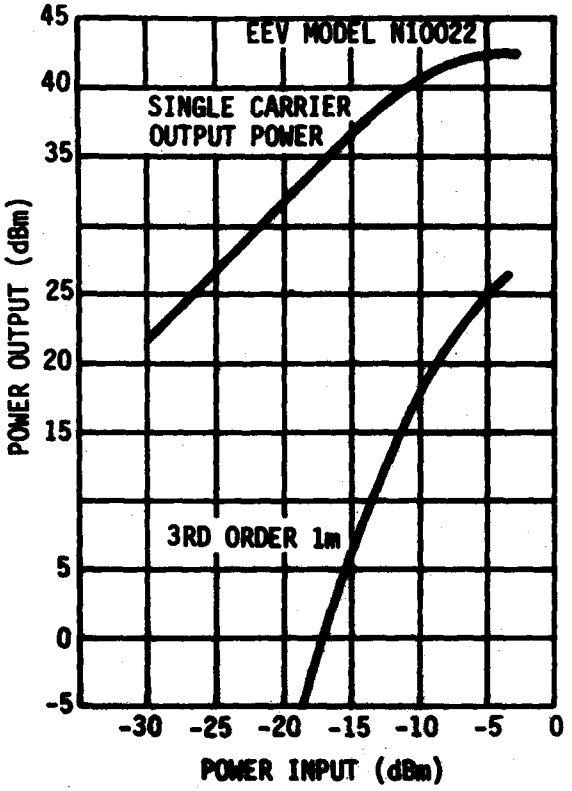

Figure 3-9. TWT AM/AM Characteristic

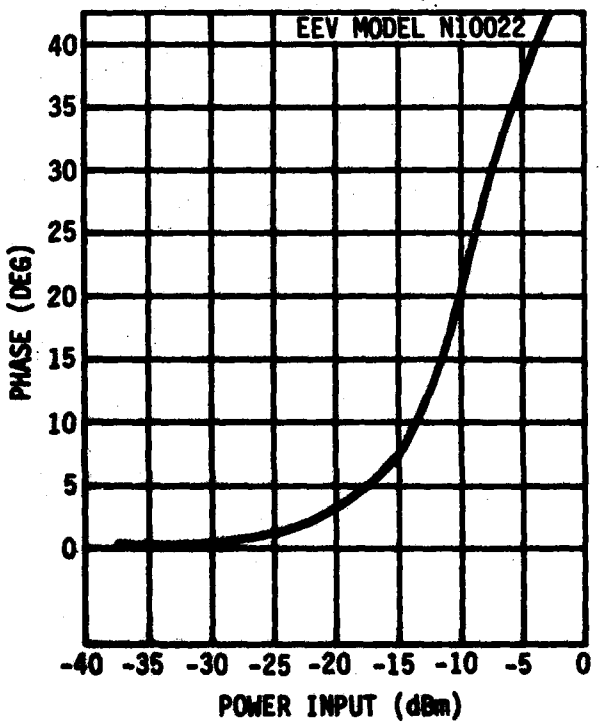

Figure 3-10. TWT AM/PM Characteristic

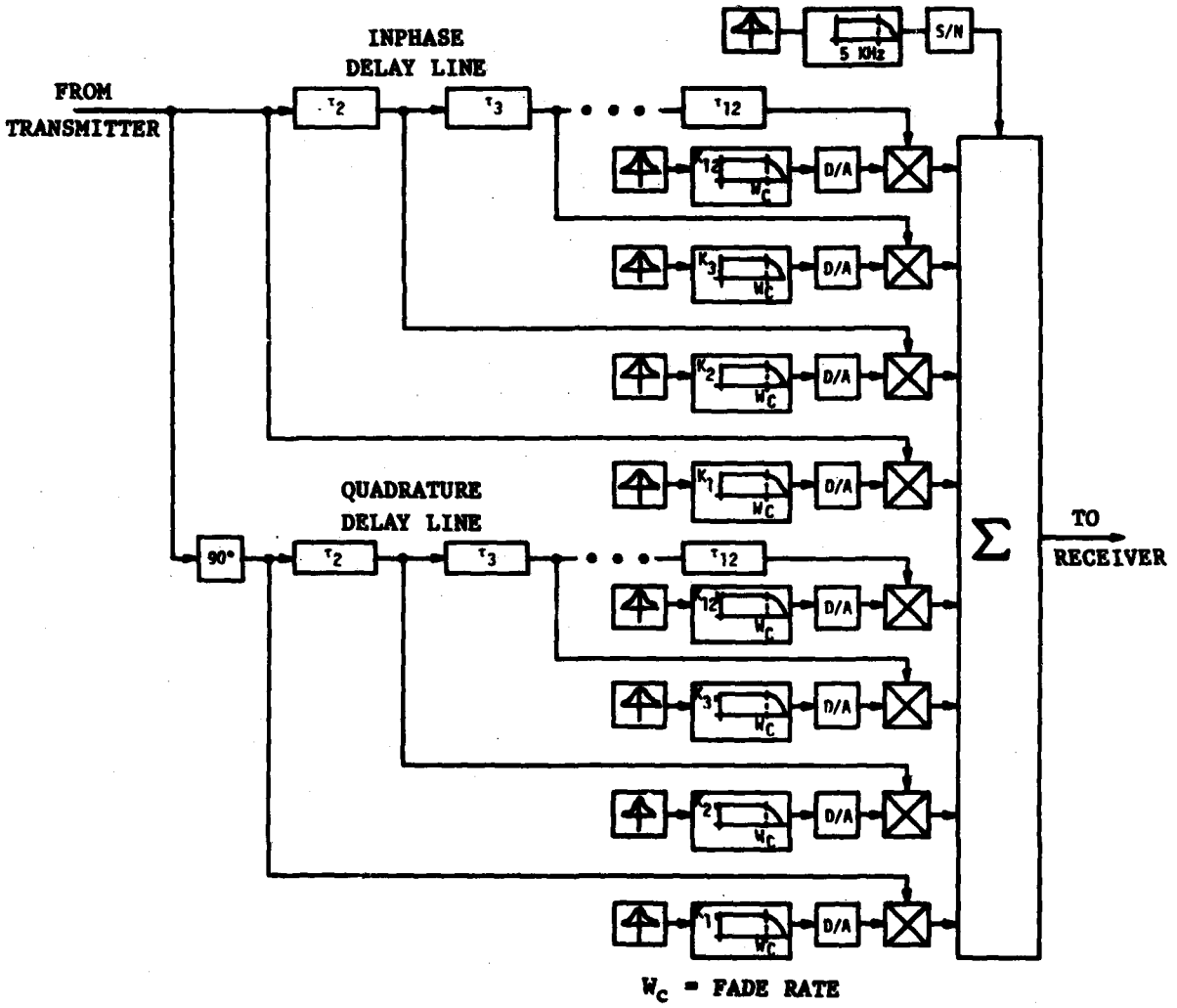

Figure 3-11. LOS Channel Model

filtered to remove sampling noise. The channel simulator has 2 delay lines, each having 12 taps. Delay line 1 is the in-phase tapped delay line, while the quadrature delay, line 2, contains an additional $\pi/2$ phase shift at each tap.

The digital filter module has been implemented on the hybrid computer system's digital computer. This computer provides the resources to generate 48 uncorrelated random noise sequences, filter them, and transfer the resulting signals to the multiplier summer module. The 48 random noise sequences were generated by sampling a Gaussian pseudo random number generator. Capability exists to provide correlation between adjacent random noise sequences by numerically combining two independent noise sources in a controlled process. The digital filters are second order Butterworth types, with a nominal cutoff frequency equal to the fade rate, with a calculated optimal sampling frequency up to 83 samples per second. The cutoff frequency can be selected by the remote hybrid terminal user at DCEC with a range between 0 and 1.0 hertz. The 48 Gaussian noise output signals from the digital filter are multiplied by the mean power coefficient at that tap, and then input to the multiplying digital-to-analog converters (MDAC) in the multiplier-summer module.

The multiplier-summer module for LOS consists of 2 channels, each of which contains 12 pairs of MDACs (1 pair per delay line tap) and a summing amplifier. One power coefficient in each pair multiplies the signal from one of the taps in delay line 1 by one of the Gaussian functions, $G_i(t)$, while the other power coefficient

multiplies the signal from the corresponding tap of delay line 2 (which is delayed an additional $\pi/2$ radians) by another Gaussian function, $G_j(t)$. The output of the 12 MDAC pairs is then summed by an analog summing amplifier network to provide the final channel output.

The LOS channel model digital program allows the simulation operator to specify the number of taps desired (from 1 to 12). In addition, enhancements were made to provide separately controllable signal to noise ratios and tap gains for each channel. A digital display and hardcopy of tap gains for both channels was provided (see Figure 4-24b) in order to allow rapid review of the channel model configuration. Options to select any tap as stationary or Rayleigh fading were also included in the model. A stationary tap was implemented from the Rayleigh fading tap by zeroing the quarature MDAC coefficient and setting the inphase MDAC coefficient to a constant value (determined from the relative mean power desired for that tap).

3.7 IF Slope and Bump Equalizer

The IF slope and bump equalizer section of the simulation compensates for the frequency selective fading effects of the channel model. The design of the unit parallels that of a similar unit described by E. R. Johnson.[2] A detailed block diagram of the model is supplied in Figure 3-12. This design corrects for $\pm$ 14 dB of gain slope across the IF bandwidth, 14 dB of notch attenuation and 6 dB of channel resonance effects.

The unit uses 5 bandpass filters of 5 MHz bandwidths each to detect spectral content in the regions centered at 58, 64, 70, 76, and 82 MHz. The detected power levels are then multiplied, or vernier-ed, by the proper constants to yield equal results in a non-frequency selective environment.

The outer two power levels, at 58 and 82 MHz, are differenced to yield an automatic gain slope equalizer control voltage. The slope equalizer acts as a constant negative slope filter with a negative control voltage input and a constant positive slope filter with a positive control voltage input. The degree of slope is controlled by the magnitude of the control voltage.

The 3 bump equalizers at 64, 70, and 76 MHz compensate for either bandpass or notch characteristics of the channel. The power level of each of the 3 mentioned center frequencies is differenced with the average of its adjacent two amplitude detection outputs. The difference is then used to drive its respective independent voltage controlled bandpass/notch filter, one of the three bump equalizers.

With a positive input voltage, the bump equalizer acts as a bandpass filter. With a negative input, the bump equalizer acts as a notch filter. The depth of notch or bandpass effect is controlled by the magnitude of control voltage.

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(2) Johnson, E. R., An Adaptive IF Equalizer For Digital Transmission; 1981 I.C.C. Proceeding, p-p 13.6.1 - 13.6.4

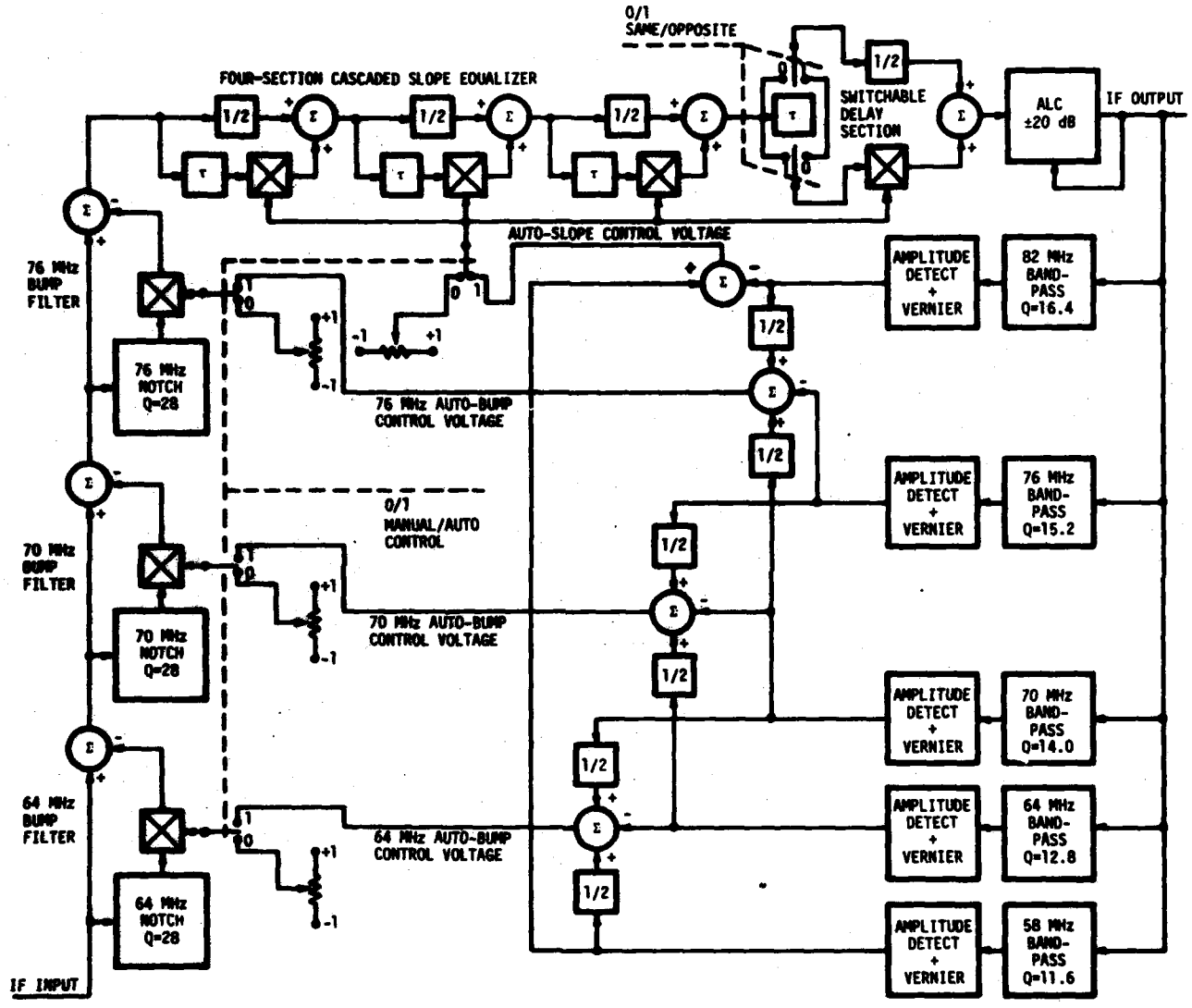


Figure 3-12. IF Slope and Bump Equalizer Model

3.8 IF Filter and AGC Circuit

The AN/FRC-170(V) dual-diversity receiver simulation was composed of two identical receiver chains. Each included an IF and AGC section, modified Costas loop demodulator, three-level detection for QPR and two-level detection for QPSK, bit timing recovery, and data regeneration. Each receiver model has an IF and AGC section that preprocesses the receiver signal from the antenna using bandpass filtering and automatic gain controls. The modeling IF filter model is a 6-pole bandpass filter with a variable bandwidth. The baseband filters were split between the receiver and transmitter, requiring a simulated IF filter bandwidth of 35 MHz. The AGC circuit controls the baseband signal level by gain adjustment to the IF signal. The real system has a dynamic range >60 dB and the modeled system has a dynamic range of 54 dB.

The simulated IF section for each receiver filters the IF signal plus noise and automatically controls the gain of the received baseband signal. Nominal values for the prototype modem's IF filter center frequency and bandwidth are 70 MHz and 40 MHz, which are 2688 Hz and 1532 Hz for the simulated filter. The IF bandpass filter simulated on the analog computer was programmed to model characteristics of Butterworth, Bessel, or Chebychev bandpass filters up to six poles. User programs have been developed to permit parameter changes for bandwidth, center frequency, ripple factor, and filter order.

The AGC circuit rectifies the IF signal and filters it with a lowpass filter to detect the IF amplitude. The error between

this amplitude and the nominal value is produced. This error is then applied to the AGC loop filter that sums the instantaneous error and integrated error as shown in Figure 3-13. This summation is the gain which the IF signal is multiplied by to achieve the nominal amplitude. The nominal value of amplitude is 25 volts. The dynamic range of the AGC circuit is 54 dB.

3.9 Modified Costas Loop Demodulator

The AN/FRC-170(V) radio uses a coherent demodulation technique which makes hard decisions on the filtered baseband and detects cross channel contamination between the I and Q demodulated symbol streams to phase lock a voltage controlled oscillator. This method of demodulation uses a modified Costas loop to extract the modulating signal. By multiplying the received IF signal with the inphase and quadrature components of the phase locked reference oscillator, the two symbol streams (I and Q) can be detected. Outputs of the I and Q phase detectors drive partial response, full cosine filters for QPR and full response raised cosine filters for QPSK. The phase lock loop uses a cross correlation between the quadrature symbol streams low-pass filter outputs and hard decision estimates to generate a phase error signal. A difference of the resulting cross correlations is filtered and input to the reference VCO to phase lock it to the modulated carrier. The data estimation circuits provide two-level decisions for QPSK and three-level decisions for QPR. Baseband filter bandwidths are set to one-half data rate for QPSK and one-fourth data rate for QPR.

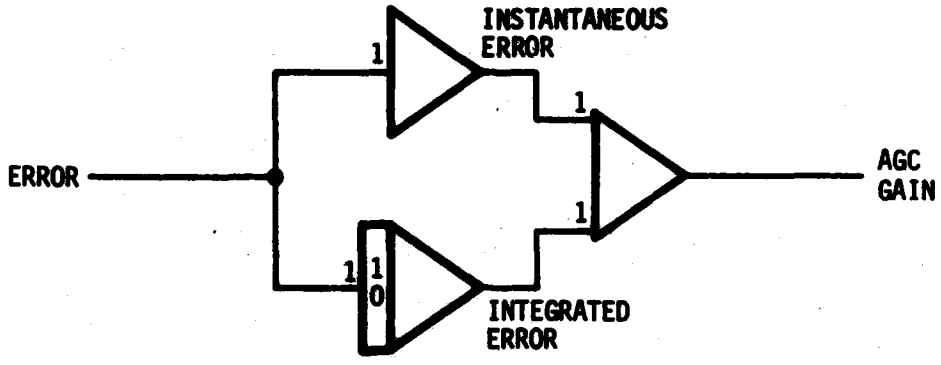


Figure 3-13. AGC Loop Filter

New design data for the carrier recovery phase lock loop filters have been incorporated into the AN/FRC-170(V) radio simulation. Separate filters for lock and acquisition modes of the phase lock loop are now selected based on the receiver's "lock" indicator. In the lock mode a narrowband filter is selected. In the acquisition mode the carrier VCO is slaved to the modulator crystal controlled VCO and a wideband filter is selected. Both the narrowband and wideband PLL filters are Type 1 second order improved types. The circuits and transfer functions of these loop filters are given in Figure 3-14.

$$H(S) = \frac{R_3}{R_1}\left[\frac{1 + SR_2C}{1 + S(R_2 + R_3)C}\right]$$

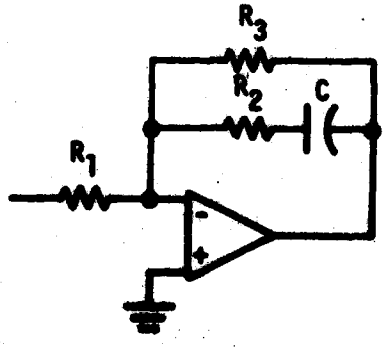


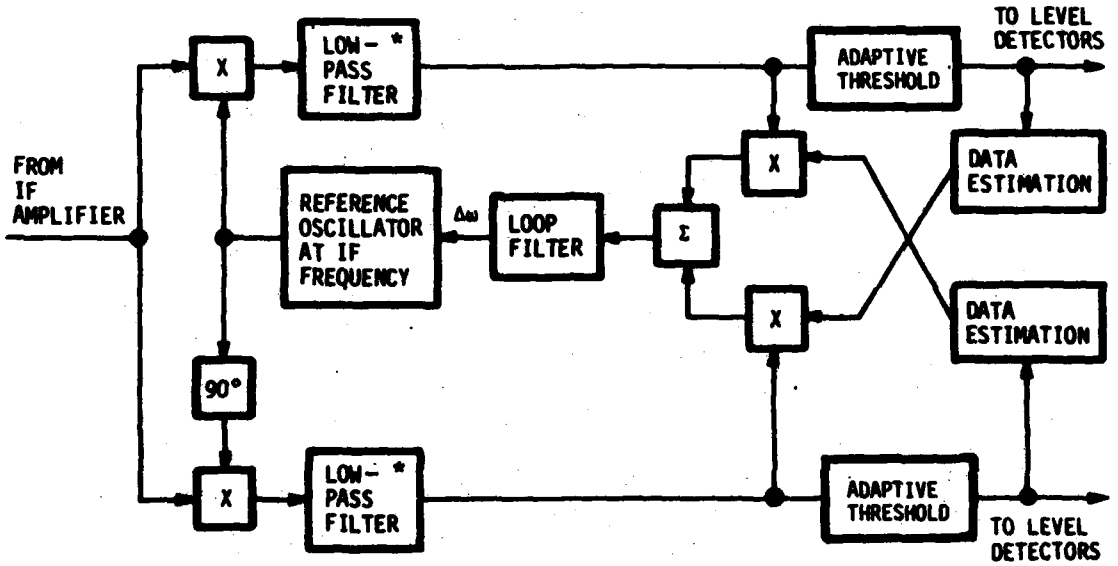
Figure 3-14. Carrier Phase Lock Loop Filter

Identical demodulators with modified Costas loops were simulated on the analog computer for each of the dual diversity receivers. This circuit coherently demodulates either QPSK or QPR transmission, depending on modulation technique selected. For QPR the low-pass filters following the phase detectors were complements to the transmit partial response filters.
The transfer function used for these filters was

$$H_r(s) = \frac{3.25104}{s^4 + 4.3966s^3 + 9.28835s^2 + 8.105s + 3.25104}$$

For the QPSK mode the filter was modified to approximate a full response with linear phase. By using a fourth order Butterworth lowpass filter, a two-level baseband signal was obtained instead of the three-level signal for QPR. The demodulator modeled on the analog computer is shown in Figure 3-15.

Phase detection of the modulating signal was simulated by using analog quarter square multipliers to multiply the received IF and phase locked reference to recover the baseband signal. Low-pass filters for the I and Q baseband data streams were mechanized similar to those described in section 3.3. These filters, partial response



*COMPLEMENT OF TRANSMIT PARTIAL RESPONSE FILTER IN QPR MODE

Figure 3-15. Demodulation Model

for QPR and full response for QPSK, filter out spurious components resulting from multiplication, leaving the difference frequency which is the baseband. These filtered baseband signals drive the data estimation circuits and cross channel I and Q multipliers. Data slicers for the data estimation and data recovery circuits were mechanized using analog comparators to determine upper and lower for QPR, and center for QPSK. Baseband adaptive threshold circuits were programmed on the analog computer and used to optimally determine slicing levels for carrier and clock threshold detecting either QPR or QPSK. The hard decisions from the data estimations of the I and Q basebands were +1, 0, -1 for QPR. Cross-coupling contamination products were obtained from the multiplication of the filtered baseband I and Q signals and an estimation of their value. The resulting signals were differenced using a summing amplifier on the analog computer and filtered by the appropriately selected narrowband and wideband PLL filters.

The optimum slicing level for data recovery, carrier recovery and the data clock is maintained using an adaptive threshold circuit. The system diagram for this circuit is shown in Figure 3-16 and the analog mechanization is shown in Figure 3-17. In the presence of noise and/or a fading channel the adaptive threshold derives an optimum slicing level by maintaining on an average a 50 percent duty cycle for the recovered clock.

The analog mechanization of the adaptive threshold was determined using reasonable approximations, of the system circuitry,

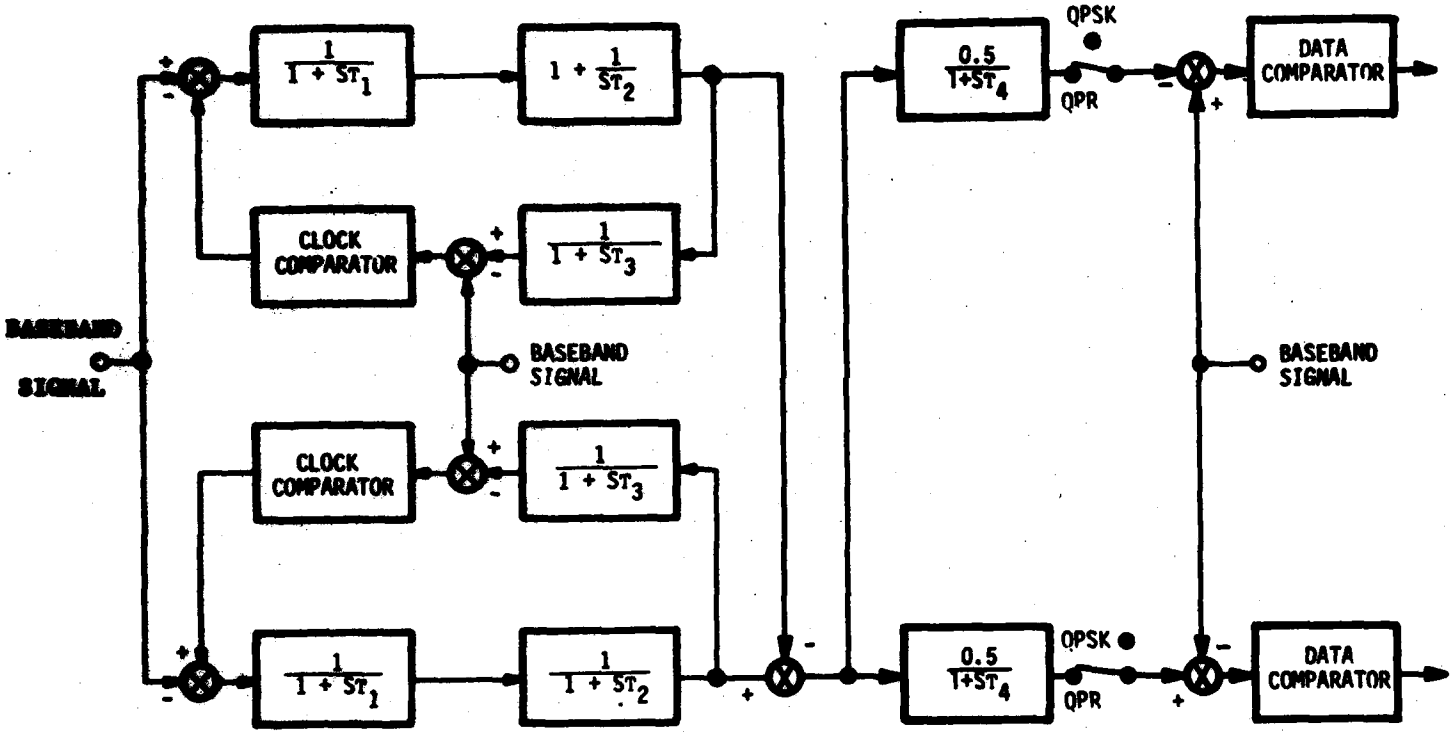


Figure 3-16. Adaptive Threshold Simulation Diagram

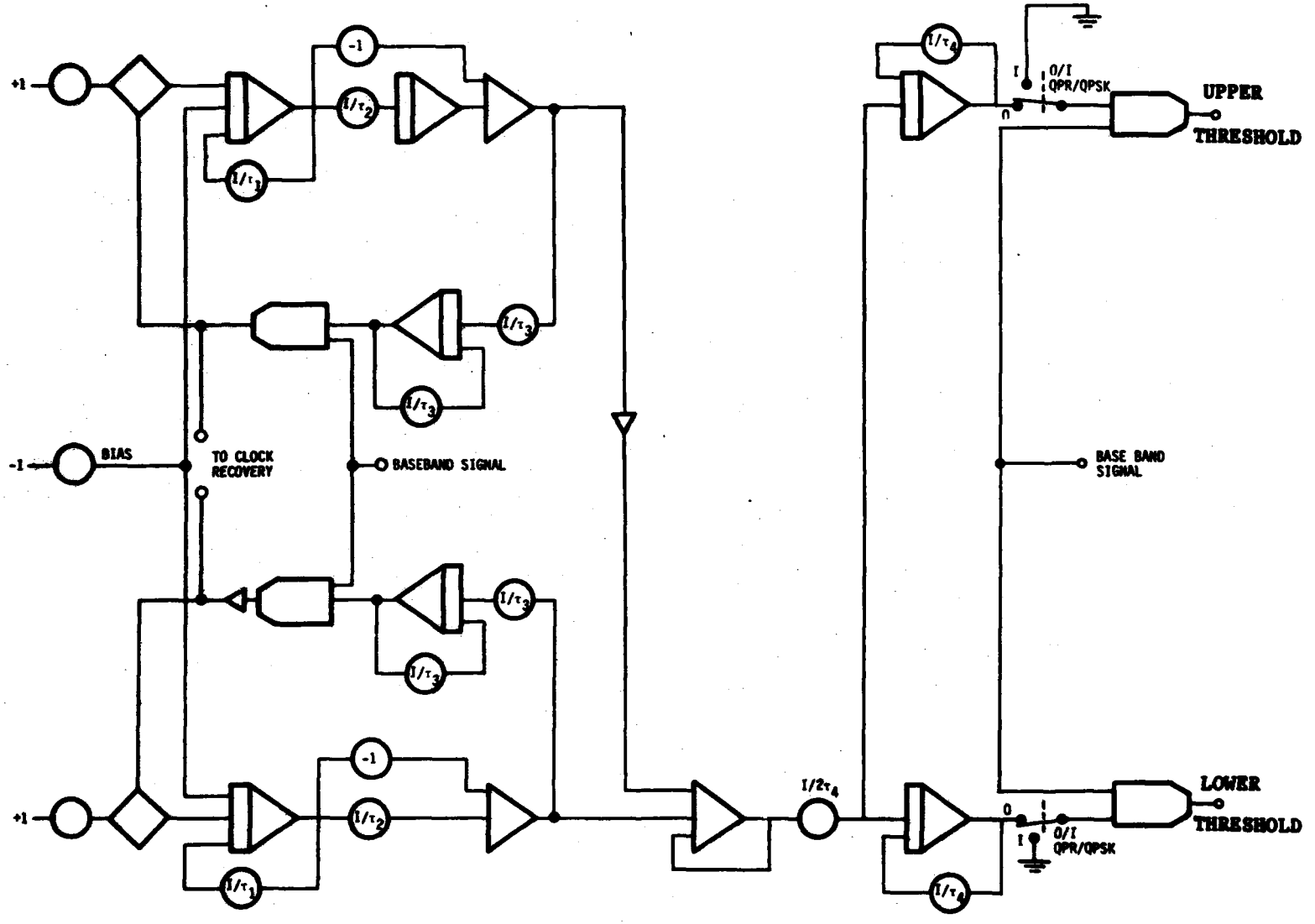


Figure 3-17. Analog Simulation of Adaptive Threshold

except for the highly coupled section that determines the data recovery slicing levels. This enhancement is based upon the actual circuit equations, thereby assuring that affects of the coupling are accurately simulated.

The narrowband, and wideband Phase Lock Loop filters were simulated as one composite filter whose time constants were controlled by the acquisition/lock detector. These filters were mechanized using analog amplifiers, electrically controlled switches, and attenuators. Nominal time constants and gain for the wideband filter were $T_1 = 29.53$, $T_2 = 0.5484$, and $A = 30.42$, and for the narrowband filter were $T_1 = 5958.8$, $T_2 = 4.178$, and $A = 26.83$. The simulation of the composite filter is shown in Figure 3-18.

3.10 Improved Baseband Equalizer Simulation

The adaptive equalizer model described in this section is implemented at the output of the QPR/QPSK demodulator. At this output either a three-level or a two-level analog representation of the baseband signal is present. Using a minimum mean squared error technique, weights for the undelayed and delayed baseband signals were generated and multiplied with the delayed demodulated I and Q analog signals. A block diagram of the baseband equalizer is shown in Figure 3-19. A block diagram showing its interaction with the rest of the radio model is shown in Figure 3-20.

This equalizer technique includes a coefficient generator that performs a cross correlation between the demodulated and equalized baseband signals, and a transversal filter that multiplies the

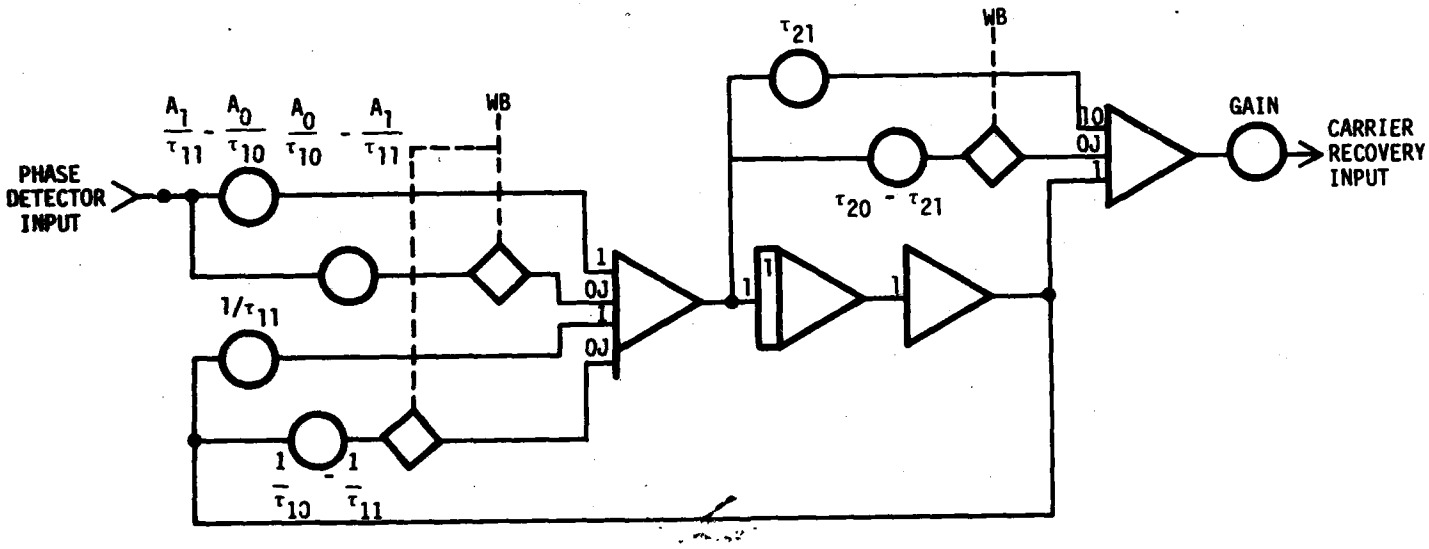


Figure 3-18. Carrier Recovery PLL Filter-Analog Simulation

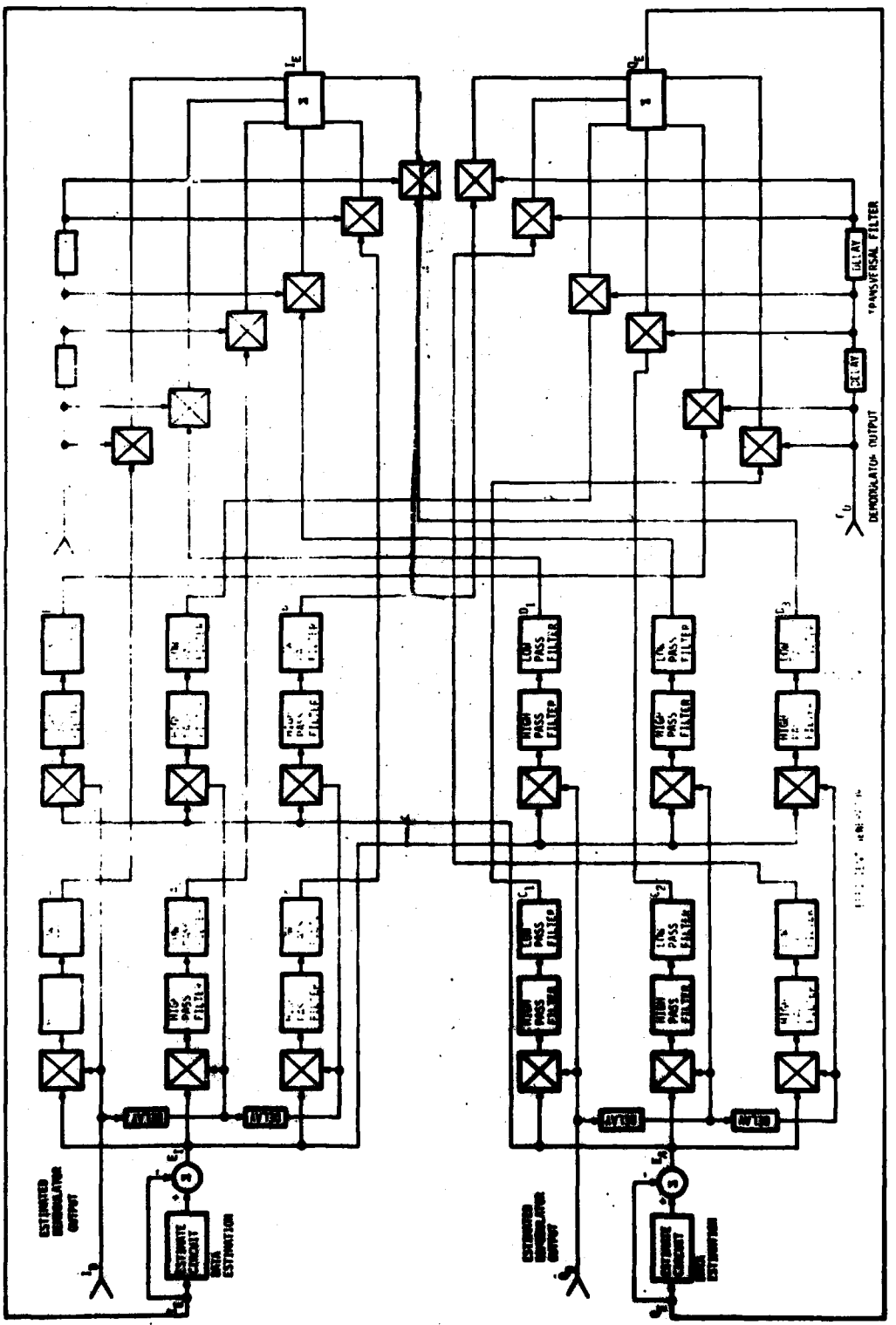


Figure 3-19. Baseband Adaptive Equalizer Model.

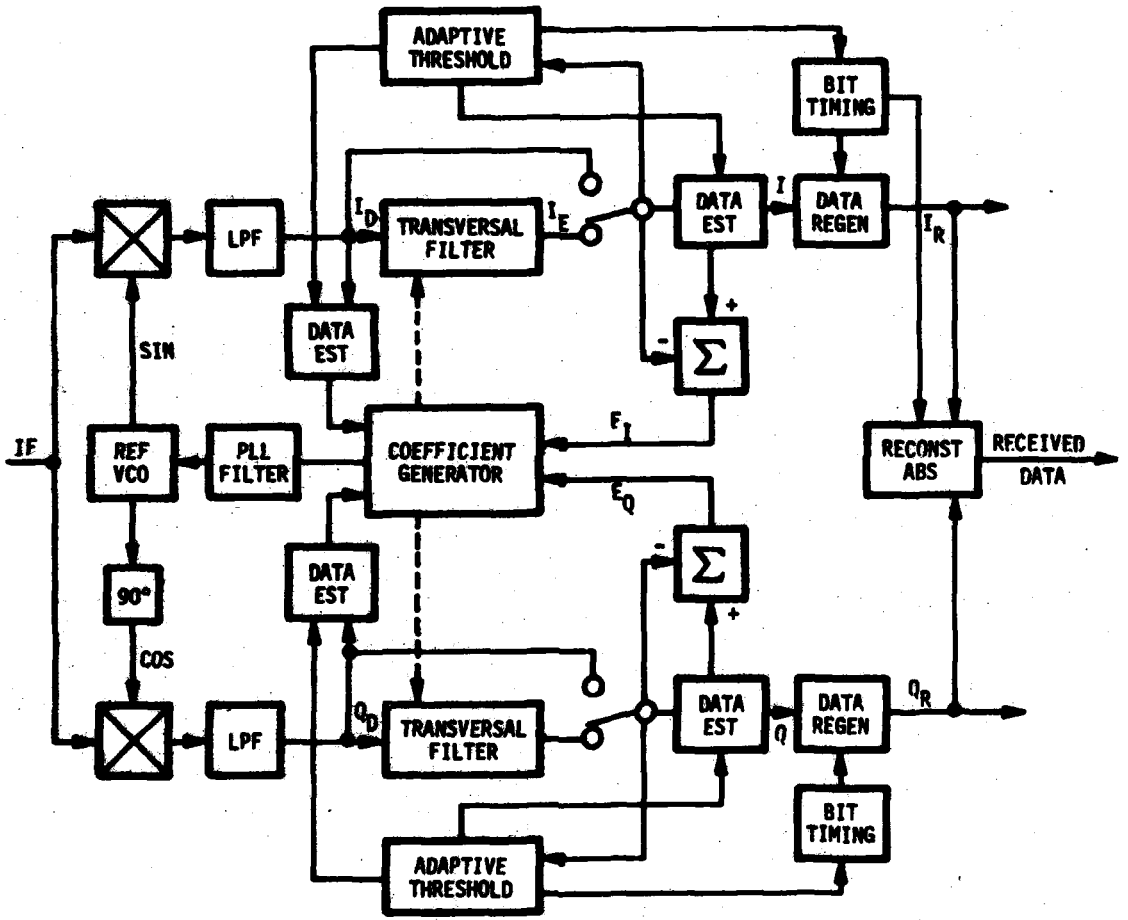


Figure 3-20. QPSK/QPR Demodulation with Baseband Equalizer

resulting coefficients and delayed demodulated baseband signals. Limiters on the inputs to the coefficient generator are required for QPSK.

Input to the coefficient generator includes the demodulated baseband signals and their respective equalizer outputs. Both the inphase (co-phasal) and quadrature basebands have associated coefficient generators. Each of these generators computes coefficients between the demodulated and equalized basebands for both channel and cross-channel errors. For example, the I channel error (coefficient) is generated by cross correlation of the demodulated I and equalized I for a given tap. The cross channel error for I is derived from the cross-correlation of demodulated I and equalized Q. Up to three taps can be accommodated using this model (one undelayed and two delayed).

The output of each correlator was high pass filtered to remove multiplier dc offset before processing by the equalizer bandwidth control filter. A bandwidth control filter for each path was mechanized using a low pass filter, with a variable bandwidth between 0.01 and 10 Hz. Twelve of these computations (or paths) are mechanized for each of the dual receivers. Up to six coefficients for both the channel and cross channel errors are computed for each receiver.

The simulation to compute one of the equalizer coefficients included a cross correlator, high pass filter, and low pass equalizer bandwidth control filter. A quarter-square multiplier was used to correlate the tap delay line input for either I or Q with the proper

equalizer I or Q output. Both filters were simulated using analog simulation techniques for transfer function simulation.

The transversal filter of the baseband equalizer performs the multiplication of each coefficient by its corresponding delayed demodulated baseband signal. For example, the equalizer output for tap 1 of the I channel was generated by summation of the products for the underlayed demodulated I, tap 1, and coefficient A_1 (cross correlation between demodulated I, tap 1, and equalized I) and coefficient B_1 (cross correlation between demodulated I, tap 1, and equalized Q). These components, representing the error (or weighting) of each tap, were summed to develop the equalized analog baseband signals. Equalizer outputs of I and Q are used as input to the data recovery circuits and as feedback to the coefficient generator.

The transversal filter incorporates two delay lines per channel (I or Q) with three taps per delay. The first tap has no delay and the second and third taps have equal and adjustable delays (usually 1 bit). The delay is controlled by an external programmable oscillator which can be set by the digital program. Custom delay line hardware has bee installed in the EAI 781 analog computers with input and output terminations available at the analog patch panel. The delay lines accept 10V p-p signal levels and have unity gain at each tap.

The delay lines were implemented using Panasonic MN3003 dual 64-stage bucket brigade devices (BBD). The MN3003 BBDs were configured for parallel-multiplex operation, therefore increasing their perofmrnace over the single stage configuration by doubling

the nyquist frequency. LM318 operational amplifiers were selected for intermediate and output stages because of their high slew rate, typically 50V/μsec. The hardware is self-supporting, requiring only a +15/-15 volt power supply and a Hewlett-Packard 3320B programmable frequency synthesizer.

3.11 Two- and Three-Level Detection

To accommodate either QPSK or QPR required both two-level and three-level detection of the baseband data. For QPR each of the demodulated I and Q baseband signals was input to the adaptive threshold circuits and combined with slicing level coefficients to form the upper and lower slicing levels. These slicing levels and the baseband signals were input to comparators for detecting the presence of +1, 0, and -1 data from the demodulated baseband signals. For QPSK, the slicing coefficients were set to zero, and only the upper comparator is used to detect the binary baseband +1, and -1. Nominally, slicing levels are set to 60 percent of peak amplitude of a baseband signal to obtain optimum detection.

3.12 Receiver Clock Recovery

The bit timing recovery circuit provides synchronization for the data recovery circuits. Separate clocks are recovered for each of the two baseband signals I and Q.

The clock comparators compare the baseband signals to threshold slicing levels which are derived from the adaptive thresholds. This comparison provides an indication of data transitions. These data transitions are exclusively or'ed with the clock outputs to produce

phase error signals. These signals drive D/A switches whose outputs are input to the phase detector amplifiers. The transfer function of the phase detector amplifier is given in Figure 3-21.

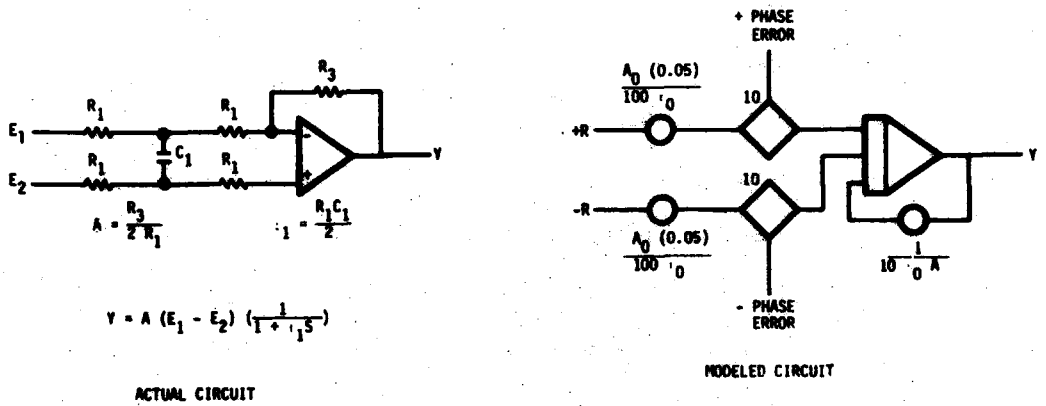


Figure 3-21. Clock Phase Detector Amplifier Model

The outputs of the phase detector amplifiers are processed by narrowband Type 2 second order filters if the carrier is in a lock state. When the carrier is in acquisition mode, a wideband Type 1 filter is electronically selected. Nominal time constants for these filters are for narrowband T_1 = 146.2 and T_2 = 47.0 and for wideband T_1 = 47.47 and T_2 = 1.295 with a gain, A = 100.56. Transfer function and circuits for these filters are shown in Figure 3-22.

The A clock output and B clock output are exclusively or'ed to provide an indication of clock synchronization. This signal drives the Sync Amplifier. When the output of the Sync Amplifier is above a set threshold a LOCK signal is produced by a difference amplifier. This LOCK signal controls the selection of wideband or narrowband clock recovery PLL filters discussed above.

The outputs of the clock recovery PLL filters are applied to the A and B clock VCO's, which drive the VCO's into frequency and phase lock with the recovered clock. A block diagram of the clock recovery loop is shown in Figure 3-23.

3.13 Data Regeneration and Descrambling

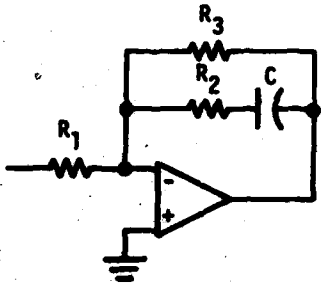
The detected two or three level baseband data is then sampled by the synchronized receiver clock for both inphase and quadrature channels. For QPR the sampling thresholds are determined by the adaptive threshold circuits. In QPSK both bit streams are then passed through differential decoders. The bit streams are then recombined to form a single serial bit stream. A 20 stage self-synchronizing descrambler is used to reconstruct the original data bit stream. A block diagram of the data regeneration and descrambling is shown in Figure 3-24.

3.14 Received Signal Level Monitor

The Received Signal Level Monitor is used to control the diversity switch and may be combined with other monitors to determine switch position. The receiver IF amplifiers are each supplied gain control multipliers at their inputs. These multipliers are driven by amplified analog signals derived from the filtered output of the AGC circuit. Using the output of this filter to drive a log function preloaded in the MFTP, a linear indicator of the received signal level (RSL) in dB is generated.

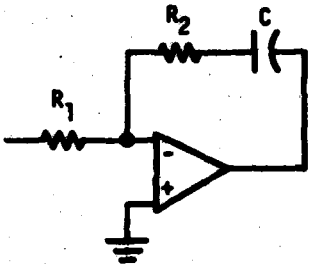
This linearity has been tested and is linear within ± 1 dB. The RSL monitor bandwidth may be varied from .001 Hz to 10 Hz by the simulation user.

$$H(S) = \frac{R_3}{R_1}\left[\frac{1 + SR_2C}{1 + S(R_2 + R_3)C}\right]$$



WIDEBAND, TYPE 1, SECOND ORDER IMPROVED

$$G(S) = \frac{1 + SR_2C}{SR_1C}$$



NARROWBAND , TYPE 2, SECOND ORDER

Figure 3-22. Clock Recovery PLL Filter Models

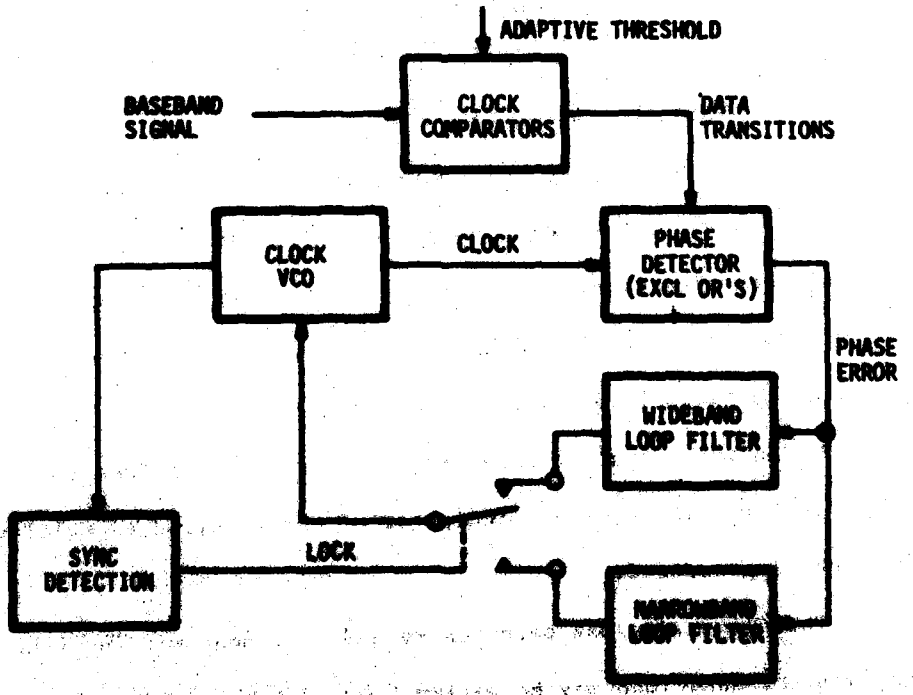


Figure 3-23. Clock Recovery Loop Diagram

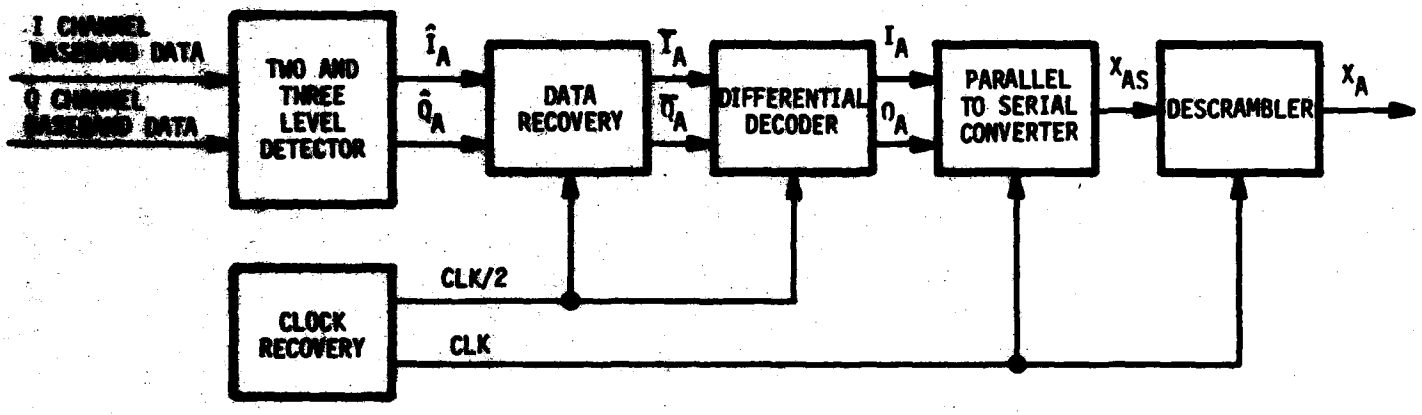


Figure 3-24. Data Regeneration and Descrambling

When using RSL as the diversity driving function, the difference between RSLA and RSLB is tested. If the absolute value of this difference is greater than an operator chosen threshold (Th2), then the receiver with the greater signal level is chosen. If the difference is less than Th2, no change in switch position is made. Th2 is nominally set at 6 dB.

3.15 Improved Signal Quality Monitor

The improved signal quality monitor is composed of two subsystems. They are the offset threshold monitor and the pseudo error counter.

The offset threshold monitor compares the baseband signal pulse amplitudes to user set acceptance ranges that are a percentage of the peak signal level. If the pulse amplitude at the time of sampling is outside of this acceptable range, then a pseudo error pulse is generated. This is shown in Figure 3-25.

α, which defines the psuedo error band, is determined by the simulation user. The Offset Threshold Monitor (OTM) user option requests the desired α from the user. This program calculates and changes the threshold levels to match the user selected α.

Threshold levels are calculated as follows:

The α given by the user is a percentage of peak pulse amplitude. This percentage is the width of an error band centered around one half of the peak value. The remaining percentage of peak amplitude is K, where $K = 1.0 - \alpha$. The lower threshold value is Peak multiplied by $\frac{K}{2}$. The upper threshold Peak is multiplied by $(1.0 - \frac{K}{2})$. This is shown in Figure 3-26.

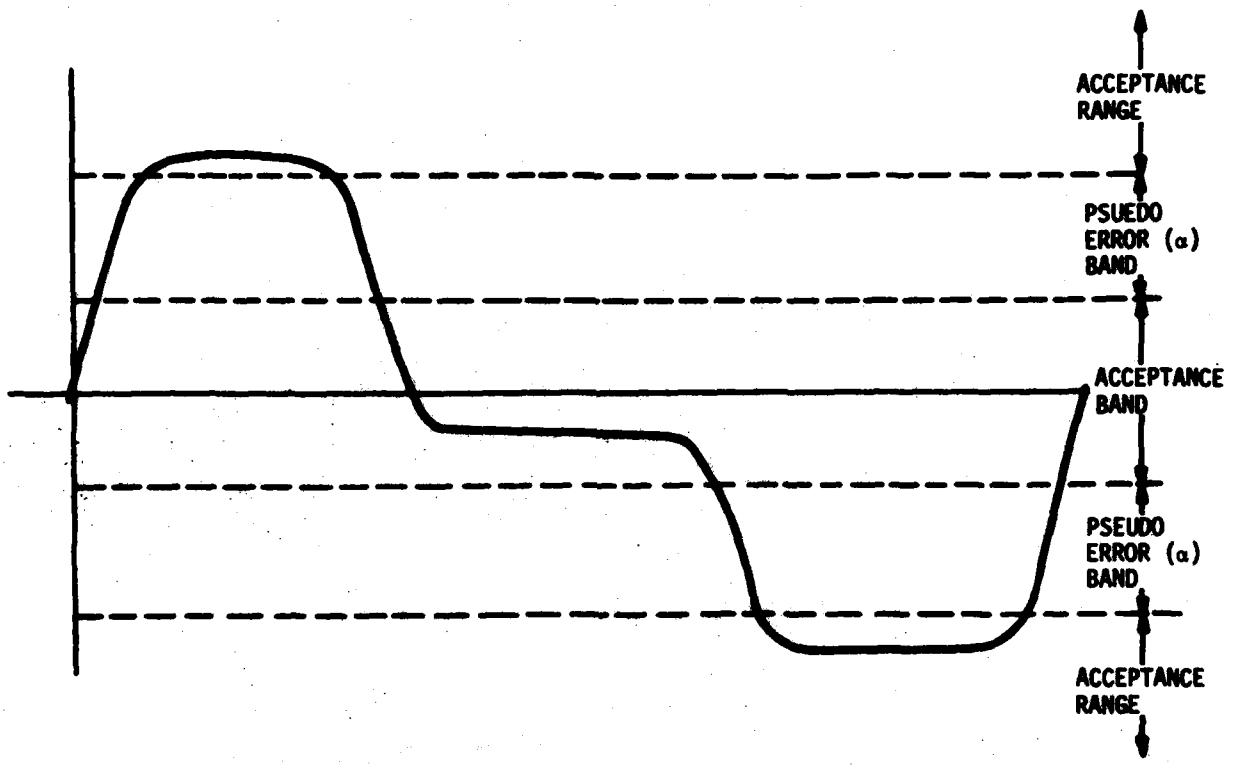


Figure 3-25. Baseband Threshold Levels

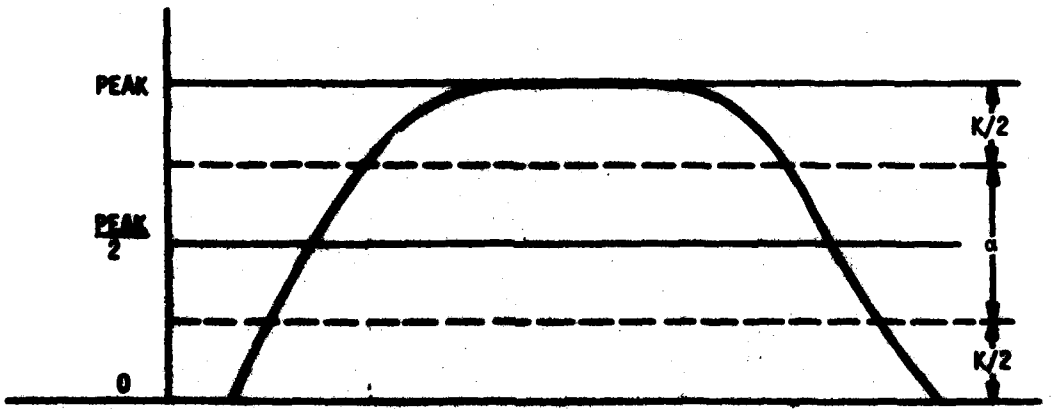


Figure 3-26. Threshold Levels for Offset Threshold Monitor

The hybrid circuitry for the offset threshold monitor is composed of comparators and logic as shown in Figure 3-27.

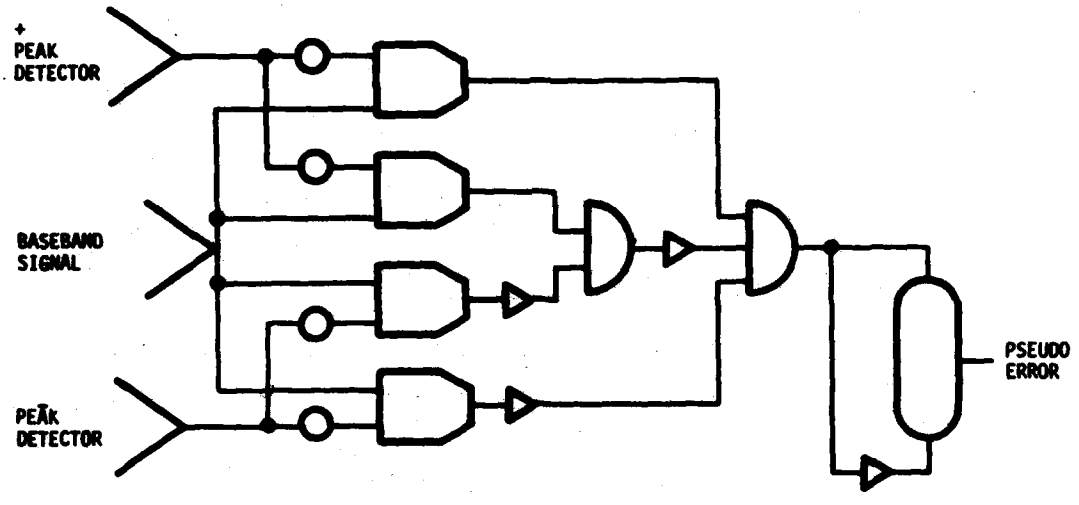


Figure 3-27. Offset Threshold Monitor Simulation

Inputs to the improved signal quality monitor are the A channel and B channel pseudo errors generated by the OTM. The diversity decision is based on the output of a digitally programmed up/down counter. Nominally counter is initially loaded with one half of its maximum count. The counter then counts up on each A channel pseudo error and counts down on each B channel pseudo error. If the counter underflows the diversity switch is set to A channel, an overflow causes the switch to change to B channel. This is shown in Figure 3-28.

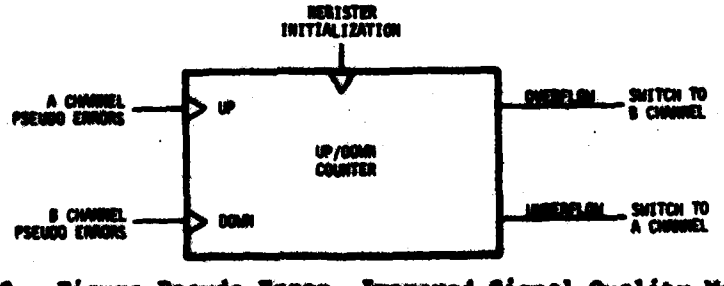


Figure 3-28. Figure Pseudo Error, Improved Signal Quality Monitor

The current counter size of the monitor is now 14 bits. A user option is available to initialize the counter to any size with 7 bits being nominal. A diversity decision flow chart is given in Figure 3-29. A hysteresis run option is now available. The user initializes the counter and receiver selection and then starts a run, which is terminated upon diversity switch. A sequence of runs can be made in this fashion with run averages made available at the end of the series.

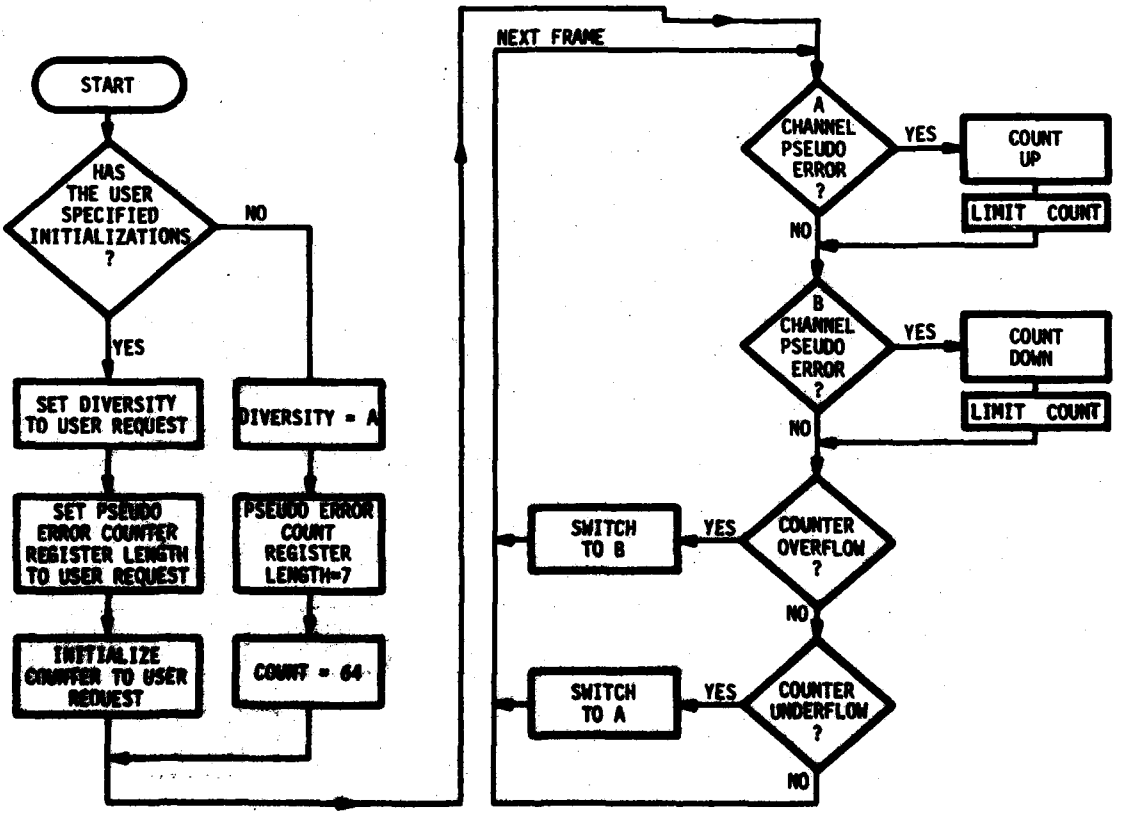


Figure 3-29. Diversity Algorithm for Pseudo Error Signal Quality Monitor

3.16 Improved Dual Diversity Selection Combiner

In the improved diversity selection algorithm two performance monitors are available as diversity driving functions. The available driving functions are received signal level (RSL) and improved signal quality monitor (SQM). Both driving function options are available in conjunction with all other simulation options.

Selection of the driving function is made by the simulation operator. Decisions made by the algorithm are dependent upon choices of threshold values also made by the operator.

The algorithm for the improved dual diversity selection is given in Figure 3-30.

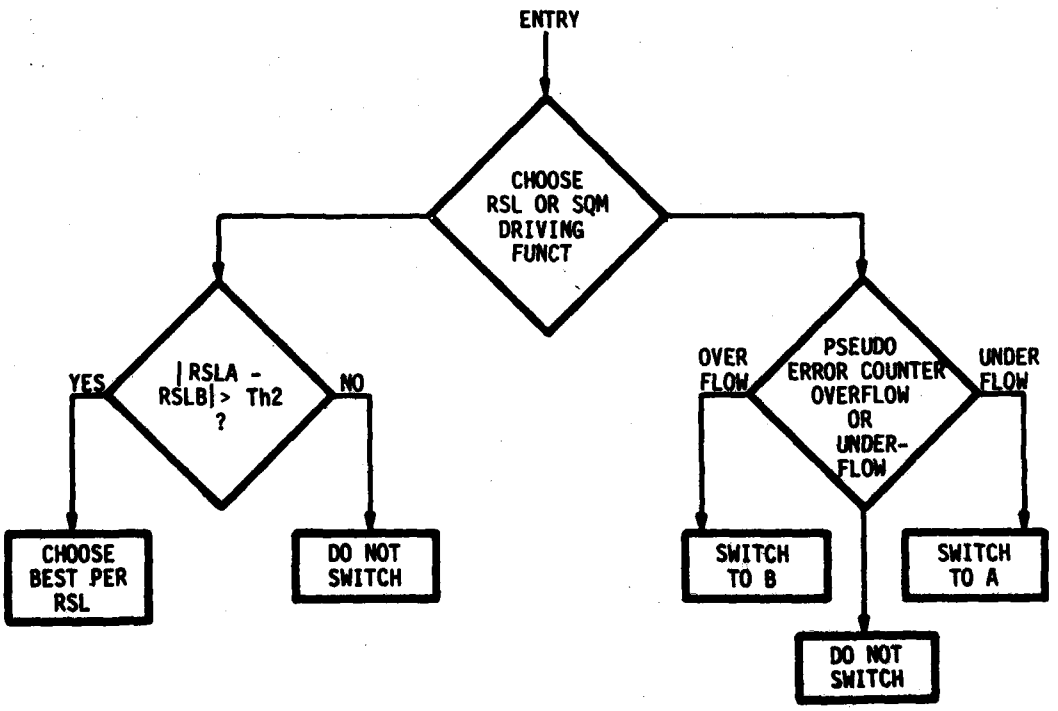


Figure 3-30. Diversity Combiner Algorithm

3.17 Fade Outage Monitor

The fade outage monitor gives an indication of percent time each receiver's signal level spends below an optional bit error rate threshold level. This threshold is selectable by the simulation user. An analog circuit measures IF signal strength in dB at each receiver. A data comparator is then used to compare the signal strength level with an adjustable fade outage threshold level for both receivers. The data comparators are then monitored each frame by the digital computer. A counter is incremented, for each reciever, each time the data comparator indicates the signal strength is below the fade outage threshold level. A third counter is also incremented every frame for a time count. Upon termination of the simulated run the percent fade outage for each receiver is computed by dividing each receiver counter value by the time counter value and multiplying by 100. Figure 3-31 shows the analog block diagram and digital flowchart for this implementation.

3.18 Bit Error Measurement

Both digital and analog computers are used in the measurement, storage, and processing of bit error data for the DRAMA radio LOS simulations. Detection of errors on a bit by bit basis is accomplished by digital processing of analog logic data.

The analog logic data for the transmitter, and both receivers consists of the transmitted and received data, clock status, and ring counter position, along with the diversity switch status. The data received by the digital computer, and a typical ring counter is down in Figure 3-32.

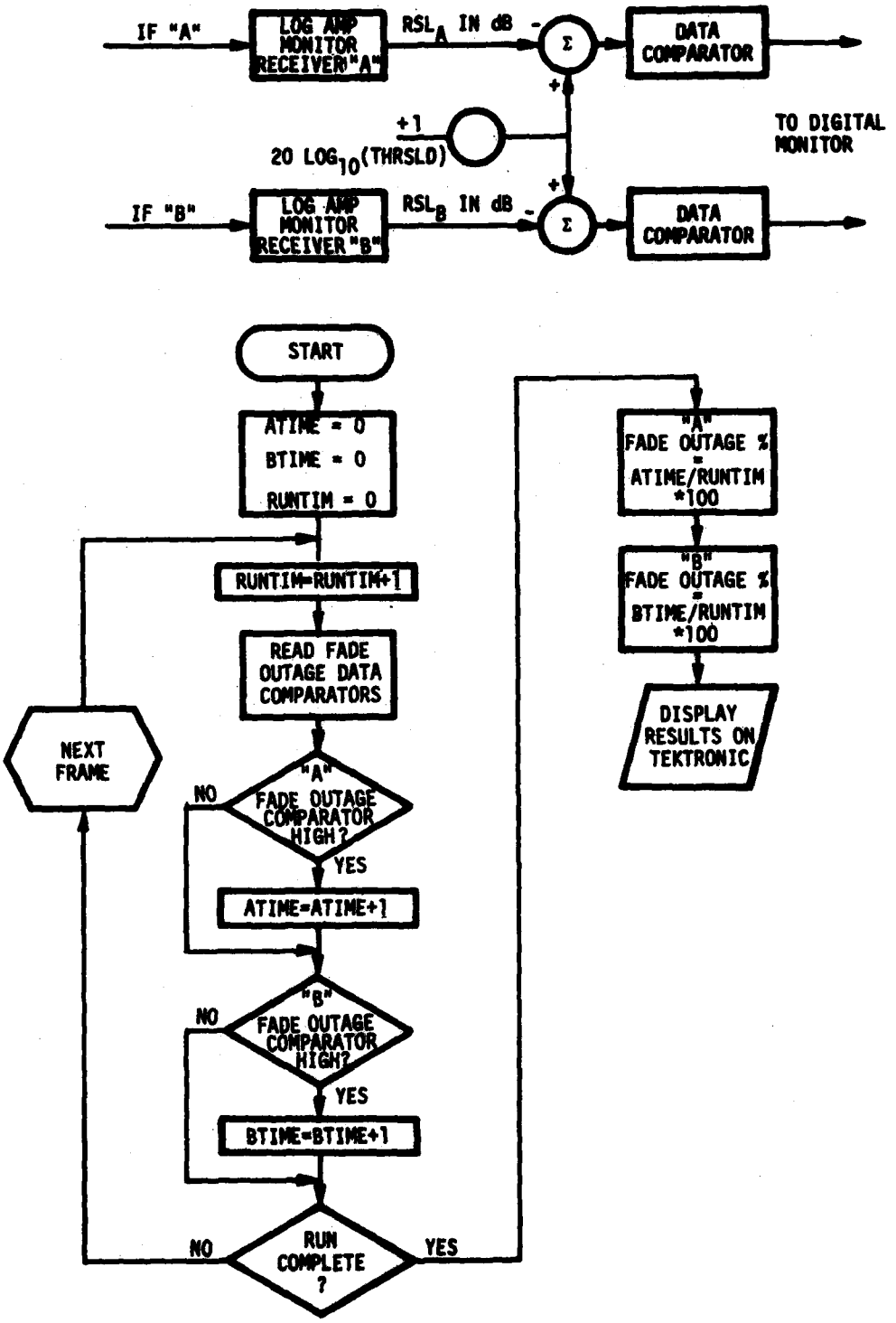


Figure 3-31. Fade Outage Monitor Simulation

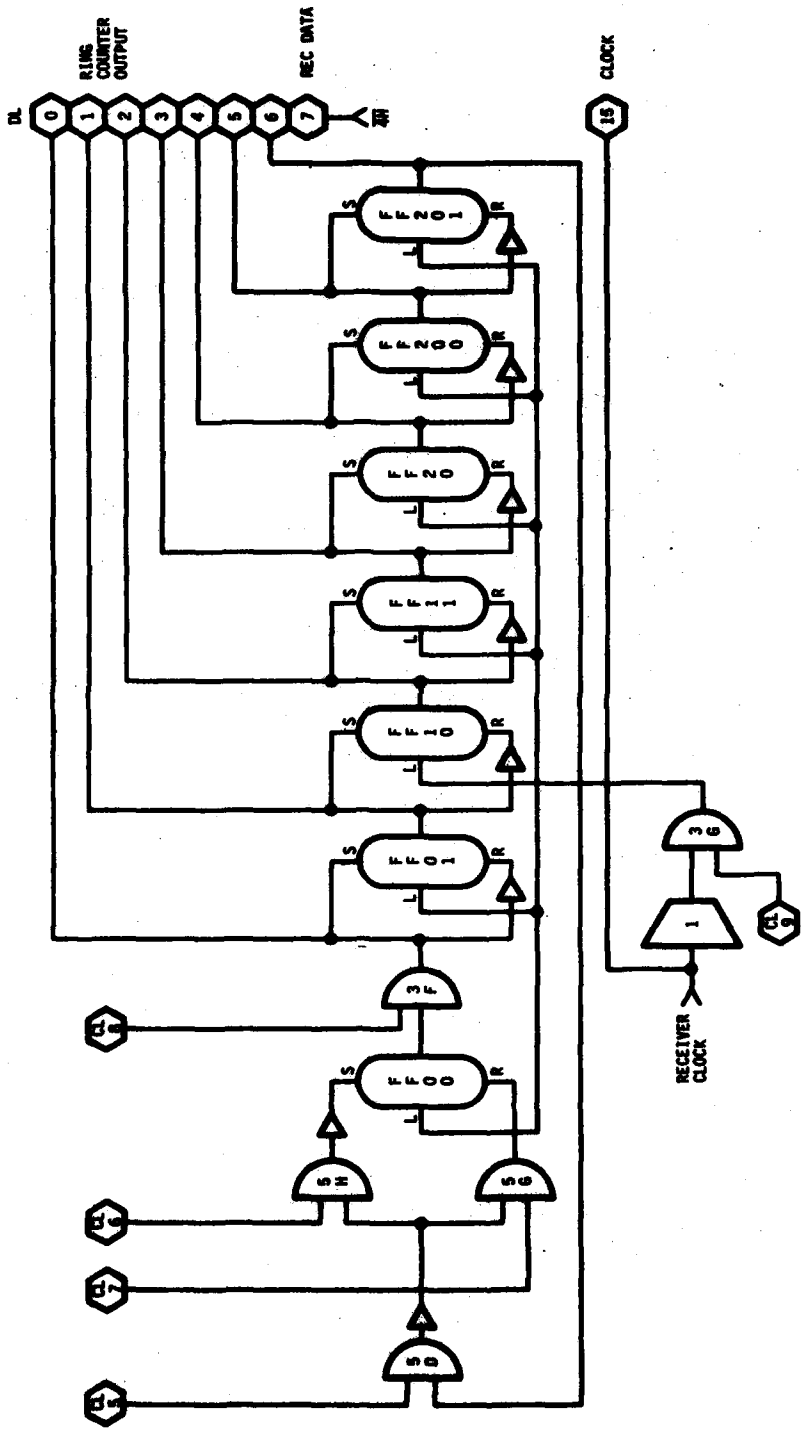


Figure 3-32. Bit Error Ring Counter Simulation

At the start of a bit error test, the channel is set to tap one stationary (the channel out condition), the ring counters are synchronized, and the transmitter and receiver bit streams are accumulated and compared to determine the transmitter receiver bit delay for each receiver.

The channel model selected is then established, the relative positions of the transmitter and receiver ring counters maintains the bit delay between the transmitter and the receiver. The desired noise level is established and the bit error test begins.

At each change of state of the transmitter clock, the data, the ring counters and clock status of the transmitter and each receiver is sampled and stored. The transmitted data is accumulated as each new bit is received, and based upon the bit delay determined through initialization and the relative position of the transmitter and receiver ring counters the correct transmit receiver bit delay is determined and the bits compared. The transmit and received clock status is used to ensure that the data has been received and the ring counters updated.

The bit errors for each receiver and the selected diversity channel are accumulated for the duration of the bit error test. These accumulated sums are divided by the current number of bits transmitted and are outputed as analog signals available for stripchart recording, thereby forming a continuous bit error rate history. The total bits transmitted, the total error for each receiver and the diversity channel, along with the respective bit error rates are reported in the Tektronix Terminal at the end of the bit error test.

4.0 HOST DIGITAL COMPUTER, ANALOG STRIPLOTS AND USER'S PROGRAM

4.1 An Overview

A significant part of the AN/FRC-170(V) hybrid radio simulation is the host digital computer. The digital computer used for this contract is a Perkin-Elmer model 8/32. The 8/32 is a 32 bit scientific machine with a 750 nsec cycle time and 0.75 M byte memory expandable to 1.0 M byte.

The 8/32 can be used in a dedicated hybrid mode, interfacing with the 4 EAI analog consoles or in a multi-terminal batch mode. When interfaced to the DRAMA modem simulation, total dedication is employed.

Some of the taks performed by the machine for the DRAMA project are, system set-up system verification, system modification, system monitoring, improved signal quality monitor activities, remote user interfacing, Fortran and assembly language program modification and overall system integration.

Section 4.7 discusses the analog stripplot capabilities.

Figure 4-1 displays how the digital interfaces with the simulation and remote user.

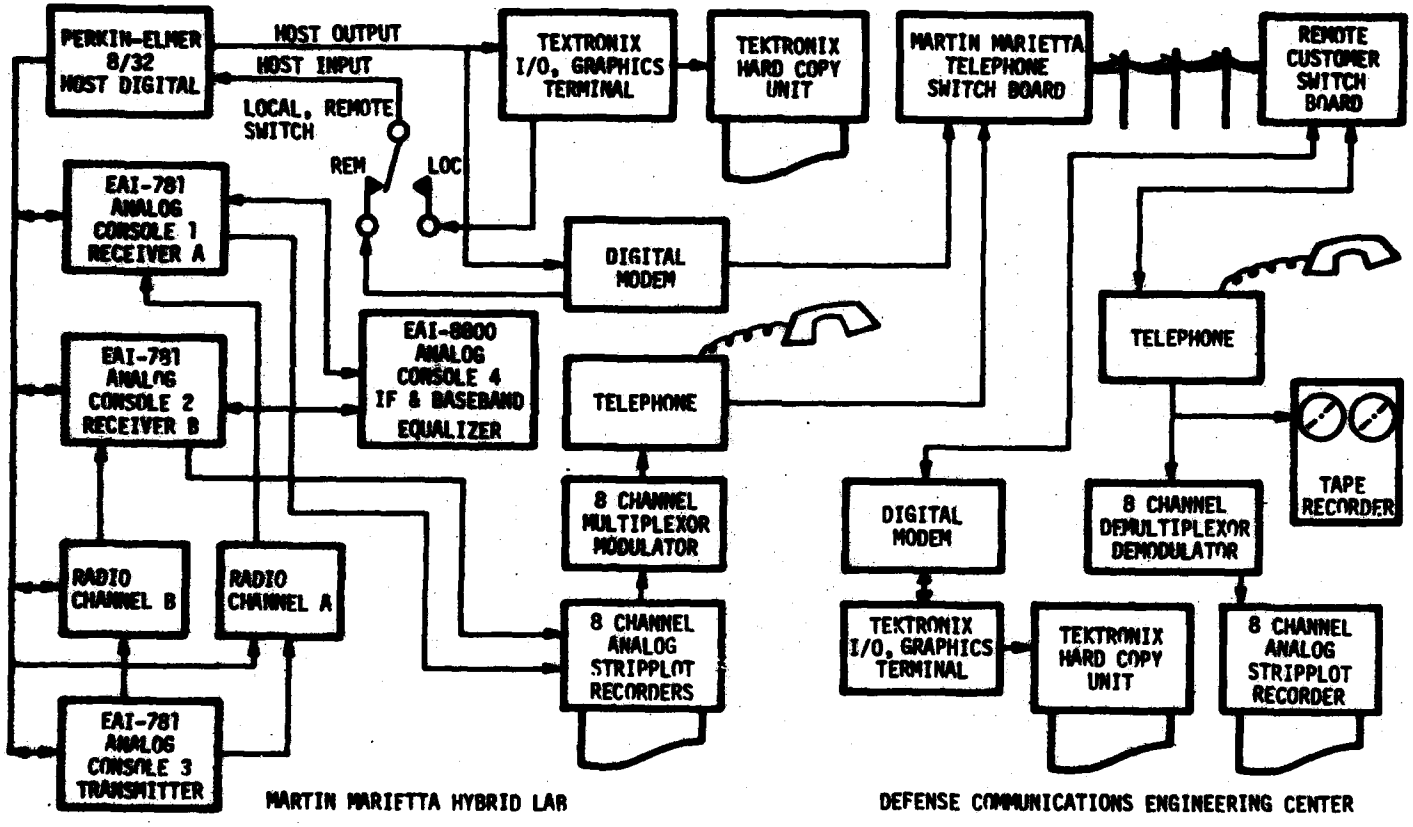


Figure 4-1. Overall System Layout

4.2 Digital Interface to Analogs - The Hybrid Link

The digital - analog interface consists of 3 main parts:

1 Analog to Digital Interface, ADCI

2 Digital to Analog Interface, DACI

3 Analog Control Interface, ACI

The ADCI consists of 32 channels of analog to 12 bit digital conversion. The main uses for the A/D interface lie in frequency response and power spectral density measurements.

The DACI consists of 80, 12 bit multiplying digital to analog convertors. DRAMA uses 48 of these to control gain and fade in the radio channel model. Reference to Figure 3-11 will show this implementation.

The pseudo error counter output is also transferred to the analog stripplot through a D/A converter.

The ACI is a general purpose interface allowing the digital to monitor and control the analog consoles.

Some of the major controlling functions include, pot setting, time scale control, logic run/stop control, logic clock control and analog mode control, (pot set, IC, hold, static test and operate). Some of the monitoring features are, pot setting verification, amplifier output readings, amplifier overflow monitoring, and logic monitoring.

4.3 The Users Program

The DRAMA digital program consists of approximately 16,000 lines of Fortran VII and assembly language. The Fortran is used in

non-real time applications to allow for ease of modification. The assembly language code is used in the real time applications such as, bit error testing, psuedo error testing, the 48 channel model digital filter updates, random number generation and diversity selection.

All of the hybrid interface functions can be commanded either through Fortran calls or assembly language calls for high speed execution. Both methods are used in the users program.

The program allows either local or remote operation.

4.4 Hybrid Computer Remote Terminal Provision

In conformance with statement of work, R220-81-011, Task 5, Martin Marietta Engineering Computing Center provides the Defense Communications Engineering Center (DCEC), Reston, Virginia, with an advanced hybrid computer terminal through which they are able to operate and control the hybrid computer simulations developed in this study. This terminal uses two telephone lines and the equipment listed below to provide stripchart analog recordings for eight channels, digital graphical displays, and control of the hybrid simulations at Orlando, Florida. The terminal equipment loaned to DCEC consists of the following items:

1. One Tektronix 4010 Terminal
2. One Tektronix 4620 Hard Copy Unit
3. One EMR Remote Terminal
4. One Eight-Channel Brush Recorder
5. One Full Duplex Telephone Modem
6. Two 1000A Data Couplers

7 One Lafayette RK-725 Cassette Tape Recorder.

The two telephone 1000A Data Couplers supplied by Martin Marietta Aerospace and installed at the DCEC facility at Reston, Virginia, are required as part of this installation to permit interchange of hybrid computer data with Orlando, Florida.

The Tektronix Terminal and hard copy units allow the customer to control the simulation and obtain results, both tabular and graphic by use of the commands described in section 4.5 and 4.6.

Figure 4-1 depicts the overall layout of the system.

4.5 User Displays and Controls

The simulation software for the hybrid simulation evaluation of frequency selective fading of DCS digital LOS radio equipment is a set of digital programs and subprograms that allow the remote terminal user to interface with the Martin Marietta hybrid computer simulation system by means of the remote terminal at DCEC. This versatile group of programs permits the remote terminal user to alter the system configuration, change system parameters, test and verify system elements, and yield sufficient data to make analytical evaluation of transmission system performance.

The Dispatch Operation System gives the remote terminal user the full flexibility of the hybrid programmer operator. Requests to the Dispatch Operating System provide access to all the program options. The majority of those are under the digital computer's control, hence are automatically integrated into the system. Some options require intervention by the hybrid operator. In this case simulation

control is returned to the hybrid operator and the remote user is requested to wait.

Input to the Dispatch Operation System is through the Tektronix graphic input terminal, and the output of the system simulation is to that terminal in the form of graphic and tabular data, and to the eight-channel stripchart recorder. The problem variables are all available for output to the eight-channel stripchart recorder. Two preset variable lists can be arranged at the time of operation such that the user may select either set. Other variables may be selected at any time to replace one or more of those in the preset lists. This is an example of a system change requiring operator intervention.

4.5.1 *Dispatch Operating System*

The transmission system simulation is changed and controlled through a set of command mnemonics. The list of common mnemonics, with explanations, is included in section 4.6. Simulation control is normally through the input command OPTN.

Receipt of the OPTN command gives a list of options available to the user. The first list is a broad classification list. Selection of an option number yields a more specific list of options. The selection of one of those causes either execution of that option or the request for necessary data and subsequent execution.

The first list is given below in Figure 4.2.

```
OPTION NO.          OPTION

   1    BIT ERROR TEST

   2    POWER SPECTRAL DENSITY

   3    RF, IF AND BASEBAND FILTER
            FREQUENCY RESPONSE

   4    RF AND IF FILTERS

   5    SYSTEM CONFIGURATION

   6    EYE PATTERN

   7    CONSTELLATION

   8    FINISHED

                    OPTION NO. =
```

Figure 4-2 OPTN Menu

4.5.2 Option 1, Bit Error Measurement

This option first requests information pertaining to the channel model to be used in the subsequent test. (See Figure 4-3)

```
CHANNEL MODEL ?
  1   OUT
  2   RAYLEIGH
  3   LOS
      OPTION NO. =
```

Figure 4-3 BITE Input Request

If the user responds with a "2", prompting for the cut-off frequencies of the Rayleigh fade characteristic occurs. (See Figure 4-4)

```
ENTER FADE RATE IN HZ FOR CHANNEL A
0.<REAL<=1.
.001
ENTER FADE RATE IN HZ FOR CHANNEL B
0.<REAL<=1
.05
```

Figure 4-4 BITE Input Request

Option 3 requires that the user previously has specified a LOS channel model profile by use of the TAP command explained in sections 4.6 and 4.5.6.3. If this has not been done, the program defaults to a single undelayed tap with no fading, which is identical to using an "OUT" channel model.

Next, the user is cued to enter the desired EB/NO for each channel and the desired run time, as in Figure 4-5.

```
ENTER EB/N0 FOR CHANNEL A
13
ENTER EB/N0 FOR CHANNEL B
8
 RUN TIME =100
```

Figure 4-5. BITE Input Request

Example inputs are provided.

At this point, the following message appears and the bit error test begins. Figure 4-6 depicts in-test display.

```
BIT ERROR TEST IN PROGRESS
PRESS <RETURN> FOR EARLY TERMINATION
```

Figure 4-6. BITE Response

As implied, the user may terminate the run before the time limitation by pressing carriage return.

The following is a typical output of a bit error run. Run time, bit count, bit error, and pseudo error count information is provided. Additionally, a total run count line is supplied in the case of a ISQM HYSTERESIS study. The following Figure is from a HYSTERESIS study providing averaged results.

```
TOTAL RUN TIME =    0.104  SECONDS
TOTAL BITS =          103

                BIT ERRORS      BER

CHANNEL A           0     3.848E-04
CHANNEL B           2     2.155E-02
DIVERSITY           2     2.039E-02

PSEUDO ERROR COUNTERS

CHANNEL A COUNT=          0
CHANNEL B COUNT=          9


NUMBER OF RUNS AVERAGED =   25
```

Figure 4-7. BITE Response

NON-OPTN INVOCATION - Type "BITE"

4.5.3 Option 2 Power Spectral Density

The Power Spectral Density (PSD) program is a hybrid technique that incorporates an analog PSD circuit that is completely controlled and sampled by the digital computer.

The hybrid circuit uses a heterodyne method of Fourier analysis to find the average power between the set oscillator frequency, and that frequency plus the bandwidth of the PSD filters.

Upon invoking the PSD option, the following list of nodes in the simulation is provided, and the user selects one. (See Figure 4-8).

```
UNIT NO.        DEVICE

   1   TRANSMITTER RF FILTER 1
   2   TRANSMITTER RF FILTER 2
   3   REC. IF FILTER CHANNEL A
   4   REC. IF FILTER CHANNEL B
   5   BASEBAND FILTER CHANNEL A-I
   6   BASEBAND FILTER CHANNEL A-Q
   7   BASEBAND FILTER CHANNEL B-I
   8   BASEBAND FILTER CHANNEL B-Q
   9    TRANSMITTER NON LINEARITY
  10   MODULATOR OUTPUT

                    UNIT NO.
```

Figure 4-8. PSD Menu

The user specifies his option and is prompted for the following input parameters, as in Figure 4-9.

```
NO. OF POINTS = 100
LOWER FREQ. IN MHZ = 20
UPPER FREQ. IN MHZ = 120
PSD FILTER BANDWIDTH IN HZ =50
```

Figure 4-9. PSD Input Request

Example inputs are provided.

In addition to the spectral occupancy plot, the program displays the upper and lower frequency bounds of the band of frequencies that contain 99 percent of the power. This 99 percent spectral occupancy is determined for the frequency extremes defined previously by the remote user. The frequency at which the center of power exists is also displayed.

Example outputs are provided in Figures 4-10 and 4-11 and also in section 5 under system verification.

NON-OPTN INVOCATION - TYPE "PSD"

4.5.4 Option 3 RF, IF and Baseband Frequency Response

This option provides the user with the capability to examine the frequency response of the eight units listed in Figure 4-12.

The frequency response program uses the outputs of the PSD circuit to digitaly compute the gain and phase of the device selected. The user is queued as to the upper and lower frequency bounds and the number of points to be tested. The program switches the output of the VCO to the input of the device being tested. At

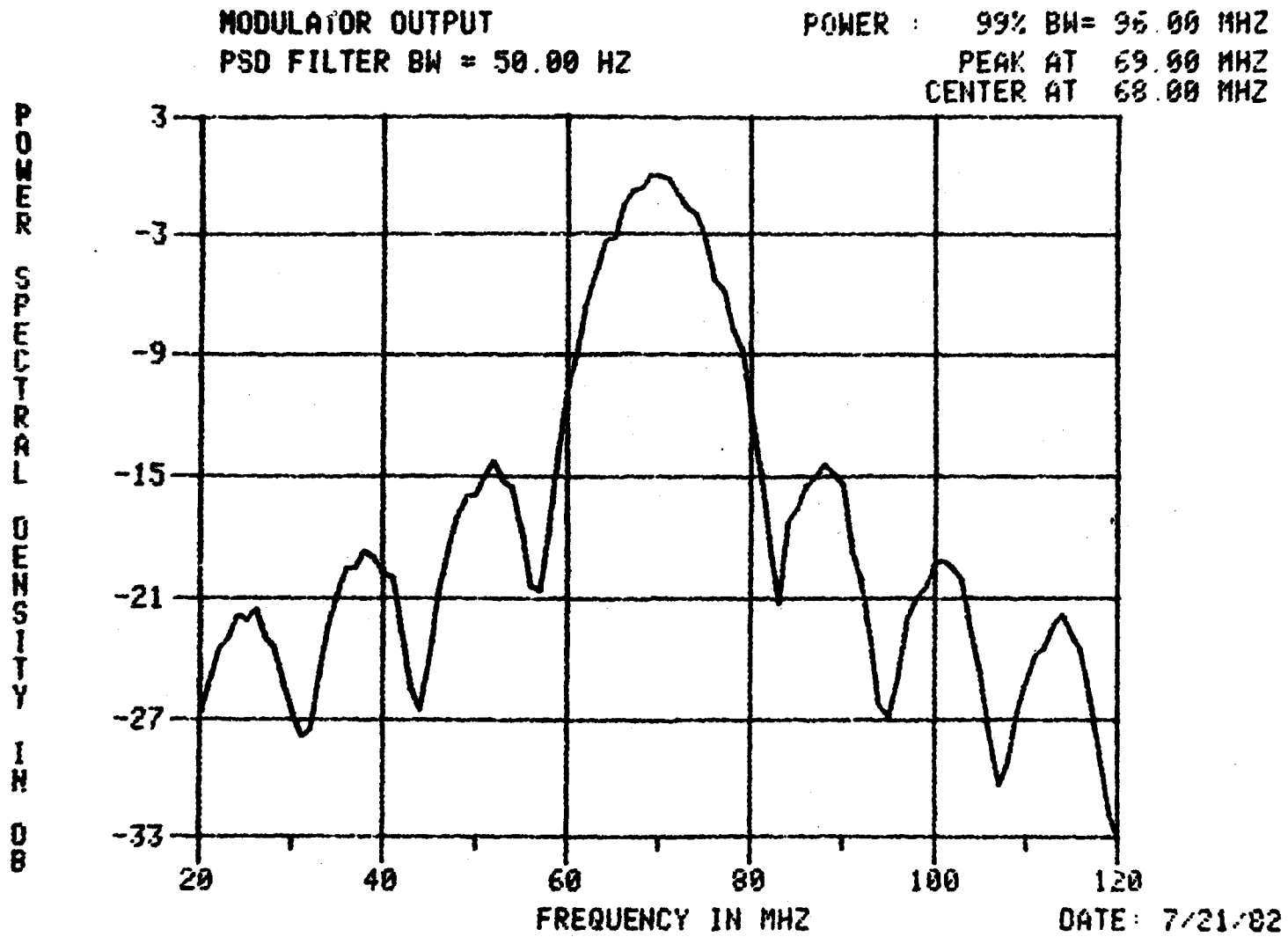


Figure 4-10. PSD Output Plot, QPSK

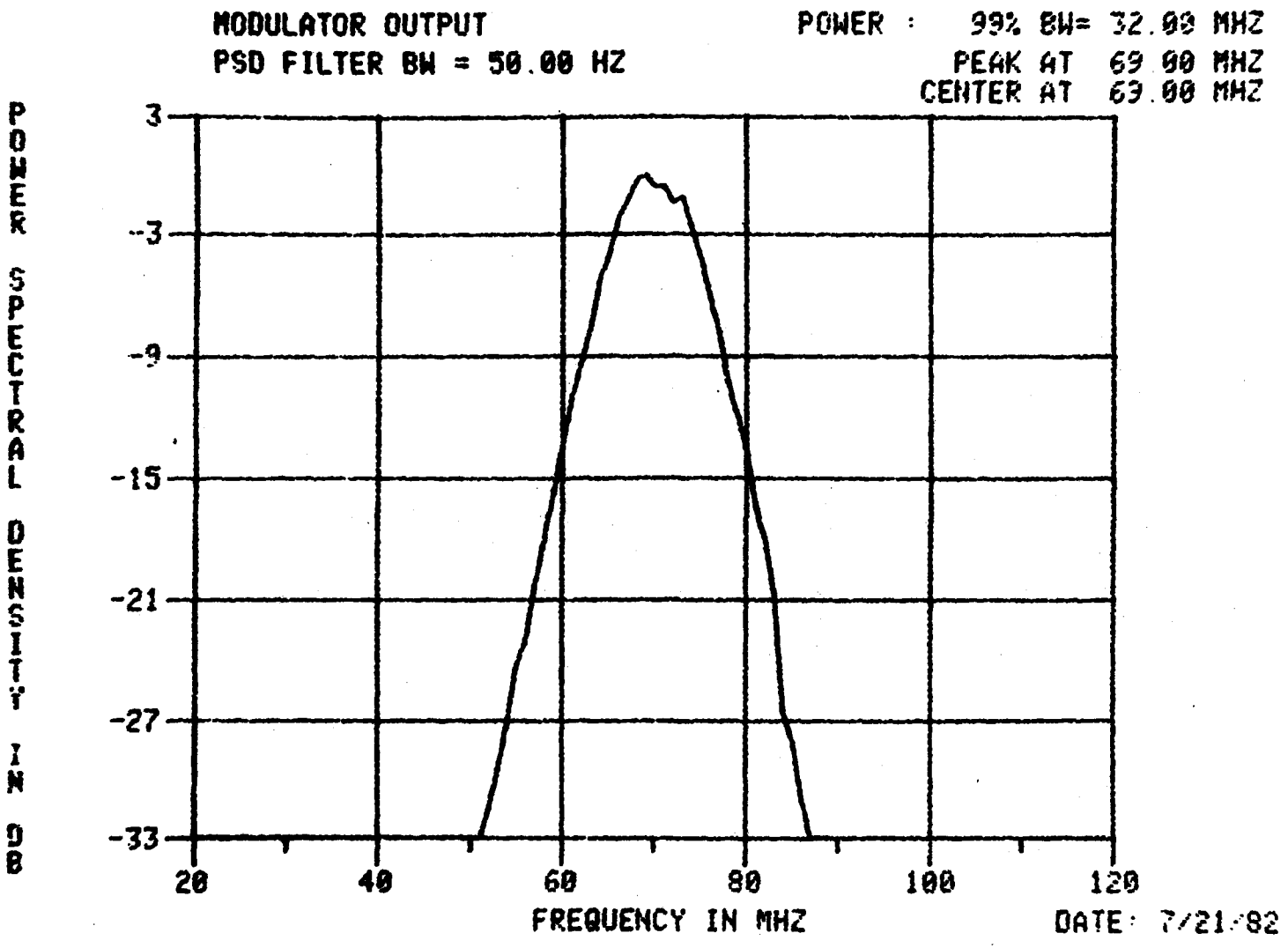


Figure 4-11. PSD Output Plot, QPR

each frequency between the upper and lower bounds, as determined by the number of points, the PSD filters are set to one-tenth that frequency, the VCO is switched to the input of the PSD circuit and the outputs are sampled, and the device is switched to the input of the PSD circuit and the outputs are sampled. The gain in dB and phase in degrees are computed.

UNIT NO. DEVICE

1 TRANSMITTER RF FILTER 1
2 TRANSMITTER RF FILTER 2
3 REC. IF FILTER CHANNEL A
4 REC. IF FILTER CHANNEL B
5 BASEBAND FILTER CHANNEL A-I
6 BASEBAND FILTER CHANNEL A-Q
7 BASEBAND FILTER CHANNEL B-I
8 BASEBAND FILTER CHANNEL B-Q

UNIT NO.

Figure 4-12. Frequency Response Menu

After selecting the desired unit, the user is prompted for number of points and lower and upper frequency bounds. (Figure 4-13)

```
NO. OF POINTS = 100
LOWER FREQ. IN MHZ = 20
UPPER FREQ. IN MHZ = 120
```

Figure 4-13. Frequency Response Input Request

Baseband and IF filter responses are supplied in Figures 4-15 and 4-16, and also in section 5 under system verification.

NON-OPTN INVOCATION - TYPE "FRS"

4.5.5 Option 4 RF and IF Filters

This option allows the user to list or change the present RF and IF filter parameters. Upon selecting option 4, the following list is displayed:

```
RF AND IF FILTERS
1  LIST FILTER PARAMETER
2  CHANGE FILTER PARAMETER
3  FINISHED
        OPTION NO. =
```

Figure 4-14. RF and IF Options

The user then specifies his selection. If option 1 is selected, the user is supplied with the type, (Butterworth, Chebyshev, or Bessel), the filter order, the passband ripple, bandwidth and center frequencies of each of the following filters:

1 Transmitter RF filter number 1

2 Transmitter RF filter number 2

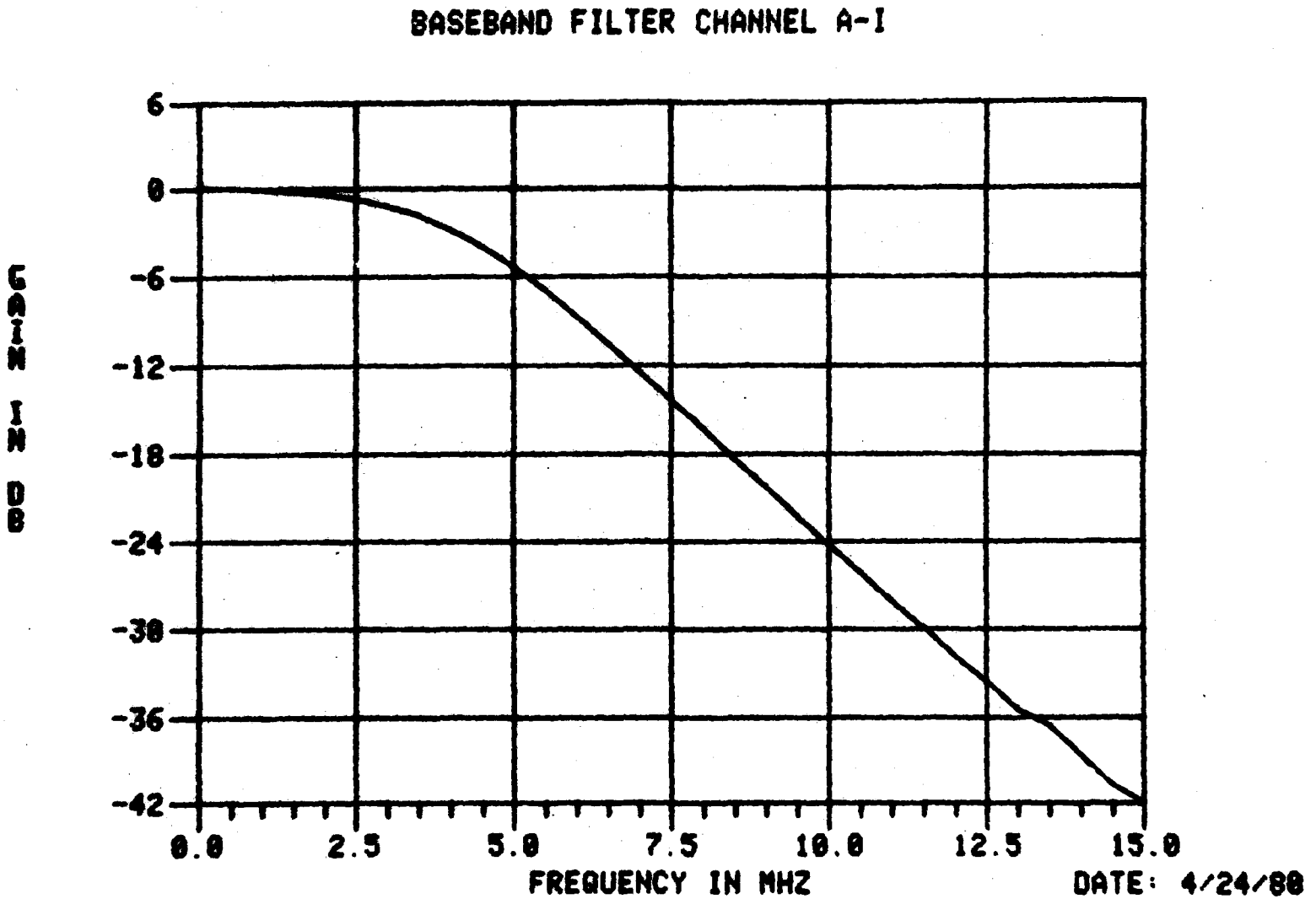


Figure 4-15. Baseband Frequency Response

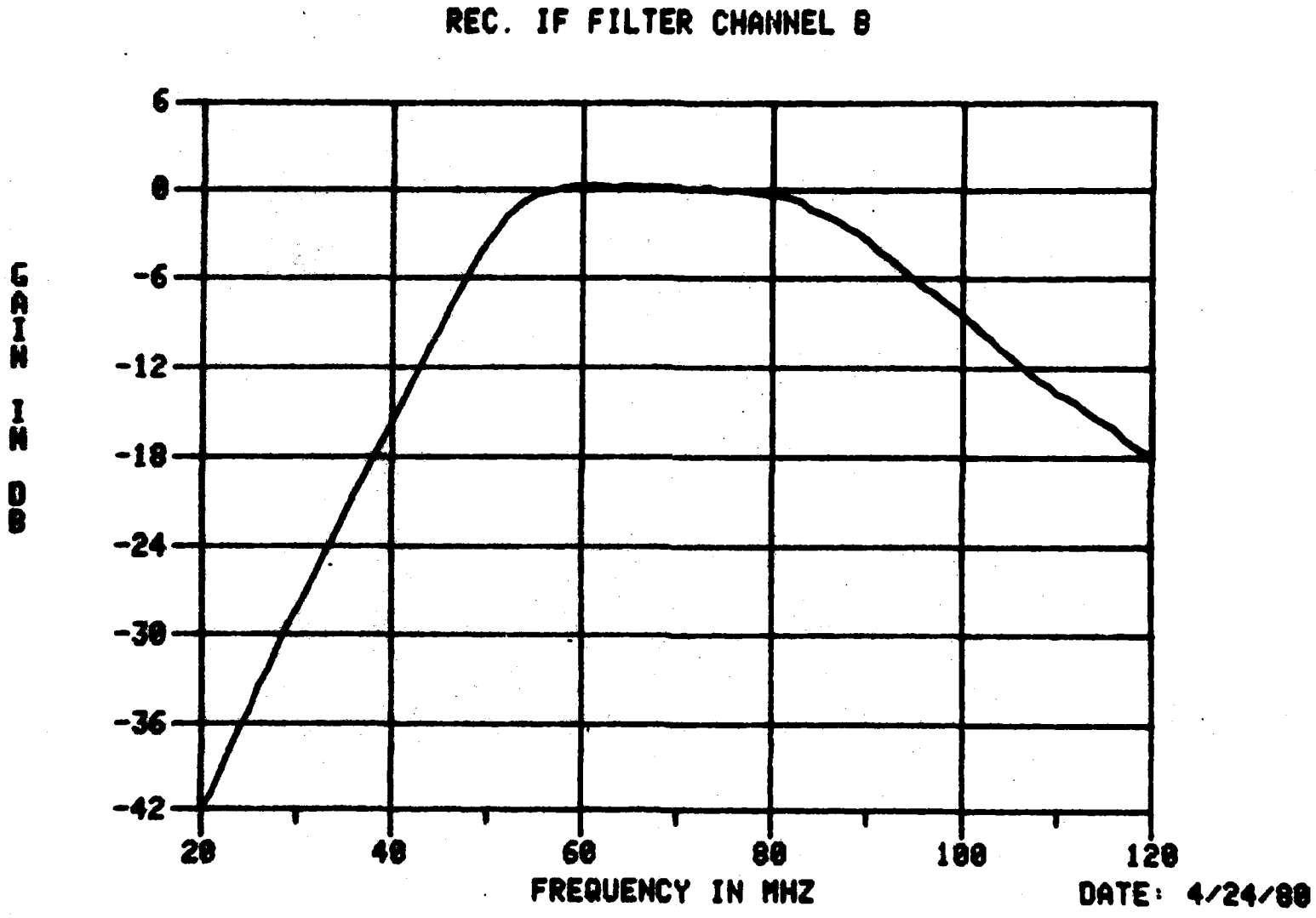


Figure 4-16. IF Filter Frequency Response

3 Receiver A IF filter

4 Receiver B IF filter.

The following is a typical listing:

```
RF FILTER NO.1
TYPE    BUTTERWORTH
ORDER                          6
RIPPLE                     0.000 DB
BANDWIDTH                 40.000 MHZ
CENTER FREQ.              70.000 MHZ

RF FILTER NO.2
TYPE    BUTTERWORTH
ORDER                          6
RIPPLE                     0.000 DB
BANDWIDTH                 40.000 MHZ
CENTER FREQ.              70.000 MHZ

IF FILTER CHANNEL A
TYPE    BUTTERWORTH
ORDER                          6
RIPPLE                     0.000 DB
BANDWIDTH                 40.000 MHZ
CENTER FREQ.              70.000 MHZ

IF FILTER CHANNEL B
TYPE    BUTTERWORTH
ORDER                          6
RIPPLE                     0.000 DB
BANDWIDTH                 40.000 MHZ
CENTER FREQ               70.000 MHZ
```

Figure 4-17. RF and IF Filter Characteristics

Alternately, the user may opt to alter the parameters of one or more of the filters by choosing option 2. The same set of filters may be altered.

Selecting option 2 produces the following list:

```
UNIT NO.        DEVICE
   1  TRANSMITTER RF FILTER 1

   2  TRANSMITTER RF FILTER 2

   3  REC. IF FILTER CHANNEL A

   4  REC. IF FILTER CHANNEL B
                        UNIT NO.
```

Figure 4-18. Filter Specification Menu

The user specifies a unit number and then is prompted for the following parameters:

```
FILTER TYPE
  1   BUTTERWORTH
  2   CHEBYSHEV
  3   BESSEL
                    TYPE =1
FILTER ORDER = 6
RIPPLE IN DB =0
BANDWIDTH IN MHZ =40
CENTER FREQ. IN MHZ =70
RF FILTER NO.1
TYPE    BUTTERWORTH
ORDER                          6
RIPPLE                      0.000 DB
BANDWIDTH                  40.000 MHZ
CENTER FREQ.               70.000 MHZ
```

Figure 4-19. Filter Specification Input and Output

Example inputs are provided.

Explanation of the RF and IF filters is provided in section 3.5.

NON-OPTN INVOCATION - TYPE "FLT"

4.5.6 Option 5 System Configuration

This option provides the user with a summary display of the simulation configuration, a means of changing the simulation configuration, and a means of setting the selected system configuration. The options within this program are listed in Figure 4-20.

The operating system maintains three system configurations. The current configuration, the nominal configuration, and the set configuration. The set configuration represents the status of the simulated transmission system. The nominal and current configurations represent two systems that are used for comparison. The set configuration is indicated in the upper right corner of the display.

Listings of the nominal and current configurations are shown in Figures 4-21 and 4-22, respectively. The current configurations is identified by number. This number is requested as part of the change configuration options.

```
                CONFIGURATION  NOMINAL

 AGC IS IN
 BANDWIDTH =  5.000 HZ


 QTM THRESHOLD
 % OF BIT AMPLITUDE = 10.00

EB/N0 CHANNELA =  12.00 DB
EB/N0 CHANNELB =  12.00 DB

CHANNEL MODEL=OUT

 RUN TIME = 10.00 SECS

 % DRIVE POWER =  99.

 DIVERSITY TECHNIQUE  AGC

 MODULATION TYPE = QPR

TRANSMITTER RF FILTER 1    IS OUT
TRANSMITTER RF FILTER 2    IS OUT

 TRANSMITTER NON LINEARITY IS OUT

 SCRAMBLER  IS OUT
```

Figure 4-21. Nominal Configuration

```
          CONFIGURATION  NO. =  2

 AGC IS IN
 BANDWIDTH =  0.200 HZ


 OTM THRESHOLD
 % OF BIT AMPLITUDE = 20.00

EB/N0 CHANNELA =  12.00 DB
EB/N0 CHANNELB =  12.00 DB

CHANNEL MODEL=OUT

 RUN TIME = 45.00 SECS

 % DRIVE POWER =  99

 DIVERSITY TECHNIQUE  ISQM

 MODULATION TYPE = QPSK

TRANSMITTER RF FILTER 1    IS IN
TRANSMITTER RF FILTER 2    IS IN

 TRANSMITTER NON LINEARITY IS OUT

 SCRAMBLER  IS IN
```

4-22. Current Configuration

4.5.6.1 **Change Current/Nominal Configuration Option**

The request input of data of the change configuration option is shown in Figure 4-23. The change configuration option does not establish that configuration in the transmission system simulation. This is done through the set configuration options that set everything except the noise level and the channel model. Noise and channel parameters are set in the bit error test subprogram.

```
 CONFIGURATION NO. =2                    TRANSMITTER NON LINEARITY IN Y/N ? N
 AGC IN  Y/N ? Y                         SCRAMBLER IN  Y/N ? Y
 AGC BANDWIDTH IN HZ =.1

 QTM THRESHOLD
 % OF BIT AMPLITUDE =20

ENTER EB/N0 FOR CHANNEL A
12
ENTER EB/N0 FOR CHANNEL B
12

 CHANNEL MODEL ?
   1   OUT
   2   RAYLEIGH
   3   LOS
       OPTION NO. =1

 RUN TIME IN SECS =45

 % OF DRIVE POWER =99

 DIVERSITY TECHNIQUE
   1   AGC
   2   ISQM
   3   HYSTERESIS
   OPTION NO. =2

 MODULATION TYPE ?
   1   QPR
   2   QPSK
     OPTION NO. =2

TRANSMITTER RF FILTER 1    IN Y/N ? Y
TRANSMITTER RF FILTER 2    IN Y/N ? Y
```

4-23. Change Current Configuration Input

4.5.6.2 Change Power Profile Option

This option allows the user to modify the channel models' individual tap characteristics. Each channels' respective power profile may be set independently of the other, or they may be set identically as an alternate option.

A typical input request is shown in Figure 4-24a with the user's responses.

The option is terminated with a listing of both channels' power profiles.

NON-OPTN INVOCATION - TYPE "TAP"

4.5.6.3 Plot Power Profile Option

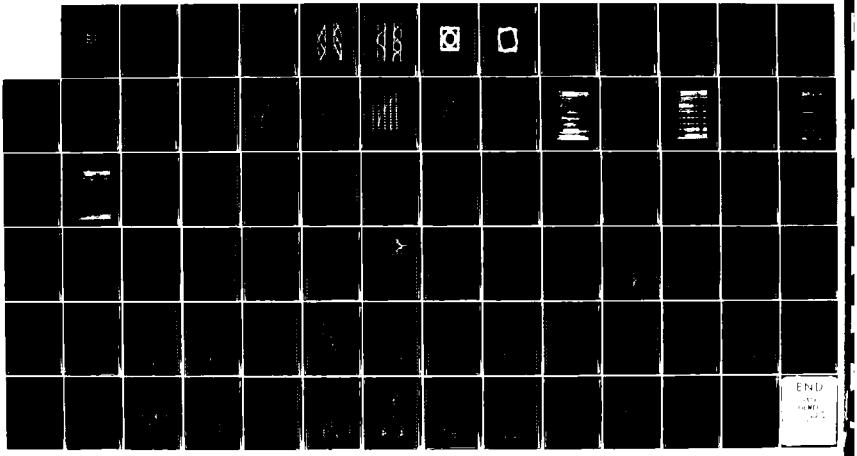
This option provides the user with a listing of both channels' power profiles. The listing generated by the input of Figure 4-24a is displayed in Figure 4-24b.

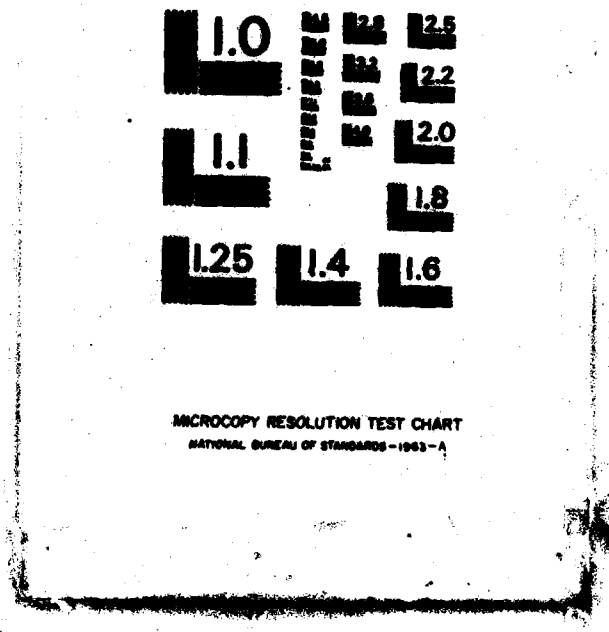
4.5.7 Option 6 Eye Pattern

This option provides the user with a display of the baseband eye patterns for inphase and quadrature modem branches. The operational system requests receiver channel, A or B, and the number of overlay plots. The inphase and quadrature baseband signals are digitally sampled 300 times with a sample time of 22.5 μs, providing a total sample time of 6.75 ms, or 3.375 symbol periods. The start of this sample period is triggered by the selected receiver clock, such that each of the overlay plots starts at the same relative time

AD-A120 816 LOS SELECTIVE FADING AND AN/FRC-170(V) RADIO HYBRID COMPUTER SIMULATION(U) MARTIN MARIETTA AEROSPACE ORLANDO FL M K KLUKIS ET AL. SEP 82 DCA100-81-C-0016 2/2

UNCLASSIFIED F/G 17/2.1 NL




1.0
1.1
1.25
1.4
1.6
2.0
2.2
2.5
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

```
IDENTICAL CHANNELS? Y/N
N
HOW MANY TAPS WOULD YOU LIKE ON
CHANNEL A      0<=INTEGER<=12
4
ENTER TAP NUMBER 1<=INTEGER<=12
1
ENTER TAP  1 GAIN.-1.<=REAL<=1.
1
FADING? Y/N
N
ENTER TAP NUMBER 1<=INTEGER<=12
3
ENTER TAP  3 GAIN.-1.<=REAL<=1.
.3
FADING? Y/N
N
ENTER TAP NUMBER 1<=INTEGER<=12
5
ENTER TAP  5 GAIN.-1.<=REAL<=1.
.05
FADING? Y/N
N
ENTER TAP NUMBER 1<=INTEGER<=12
7
ENTER TAP  7 GAIN.-1.<=REAL<=1.
.063
FADING? Y/N
N
CHANNEL A INPUT COMPLETE
HOW MANY TAPS WOULD YOU LIKE ON
CHANNEL B      0<=INTEGER<=12
2
ENTER TAP NUMBER 1<=INTEGER<=12
1
ENTER TAP  1 GAIN.-1.<=REAL<=1.
1
FADING? Y/N
N
ENTER TAP NUMBER 1<=INTEGER<=12
4
ENTER TAP  4 GAIN.-1.<=REAL<=1
.04
FADING? Y/N
N
CHANNEL B INPUT COMPLETE
```

Figure 4-24a. Channel Model Input

CHANNEL MODEL POWER AND FADE RATE PROFILES

CHANNEL A PARAMETERS				CHANNEL B PARAMETERS			
TAP	GAIN	TYPE	FADE RATE	TAP	GAIN	TYPE	FADE RATE
1	1.000	STAT		1	1.000	STAT	
3	0.300	STAT		3	0.000	STAT	
4	0.000	STAT		4	0.040	STAT	
5	0.050	STAT		5	0.000	STAT	
7	0.003	STAT		7	0.000	STAT	
RAYLEIGH CUTOFF FREQ.			0.000 HZ	RAYLEIGH CUTOFF FREQ.			0.000 HZ

Figure 4-24b. Channel Model Output

within the symbol period. Typical eye patterns for QPR and QPSK modulation are shown in Figures 4-25 and 4-26.

NON-OPTN INVOCATION - TYPE "EYE"

4.5.8 Option 7 Constellation

This option provides the user with a display of the receiver's baseband constellation. The operational system requests the receiver channel, A or B, and the number of overlay plots. The inphase and quadrature baseband signals are digitally sampled 1000 times at a sample period of 22.5 μs. These samples are plotted using the inphase data as the horizontal axis, and the quadrature data as the vertical axis. Constellations for QPR, channel out, and QPSK for channel in, are shown in Figures 4-27 and 4-28, respectively.

NON-OPTN INVOCATION - TYPE "LIS"

4.6 NON-OPTN Command Mnemonics

The DRAMA program can be run in a non-OPTN mode where the user types in a single short command mnemonic to initiate any of the OPTN options. There are also a number of command mnemonics which allow options not obtainable through the OPTN dispatch routines.

The command mnemonics permit the user to go directly to the desired result which is usually a quicker and more efficient process than sub-opting through OPTN.

Any of the entered command may be nullified prior to the final carriage return by depressing the keyboard "CTRL" key and "B" simultaneously.

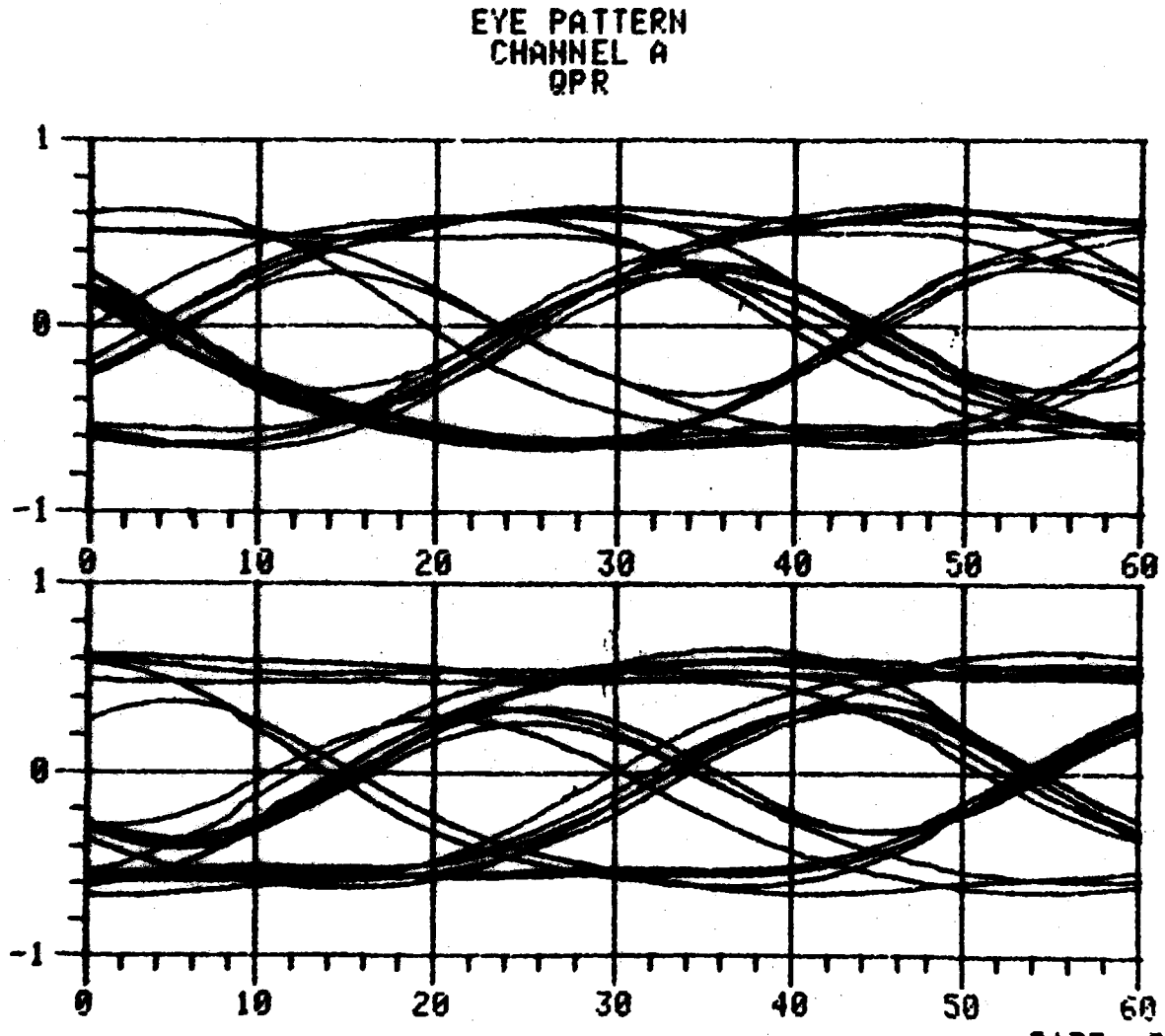


Figure 4-25. QPR Eye Pattern

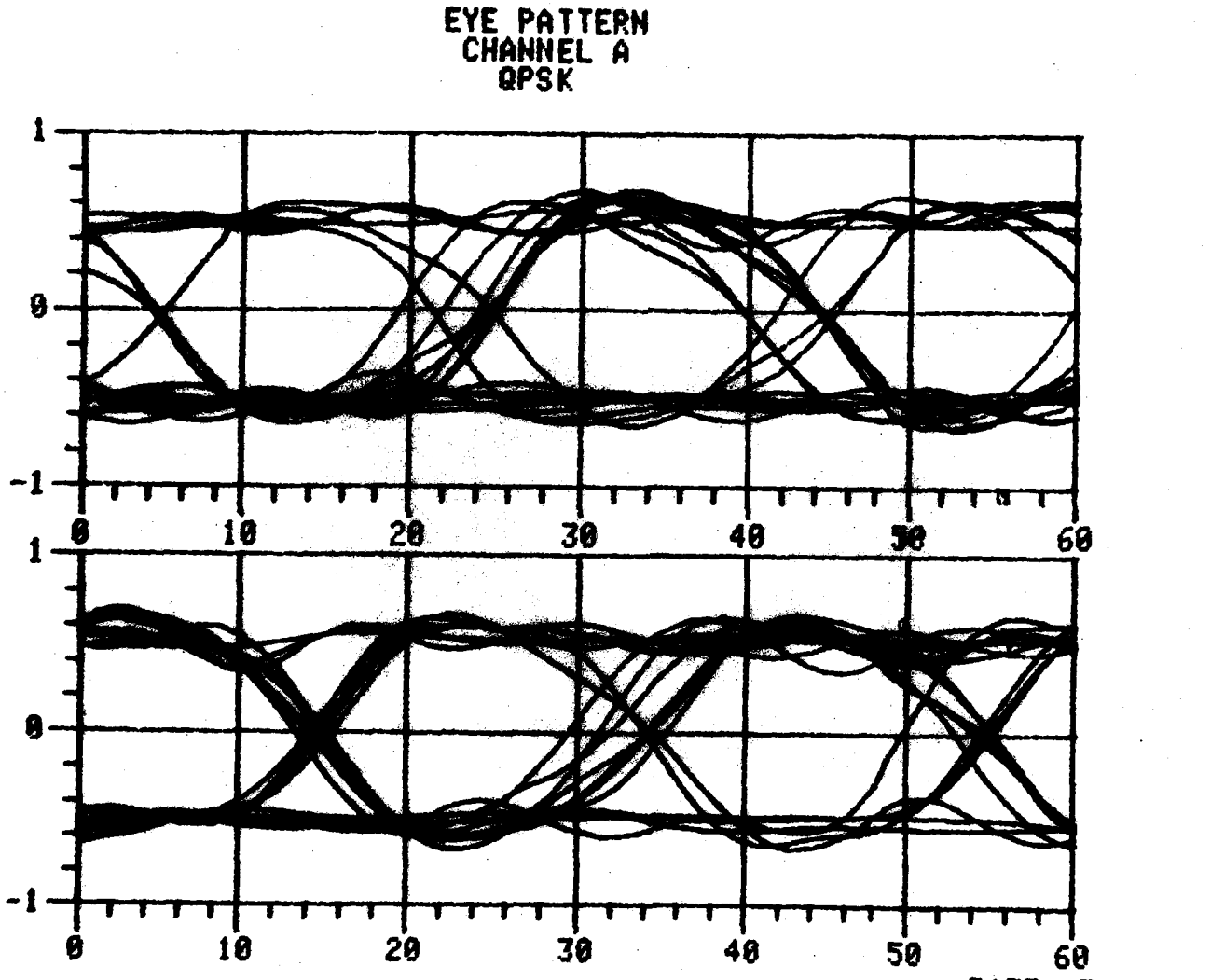


Figure 4-26. QPSK Eye Pattern

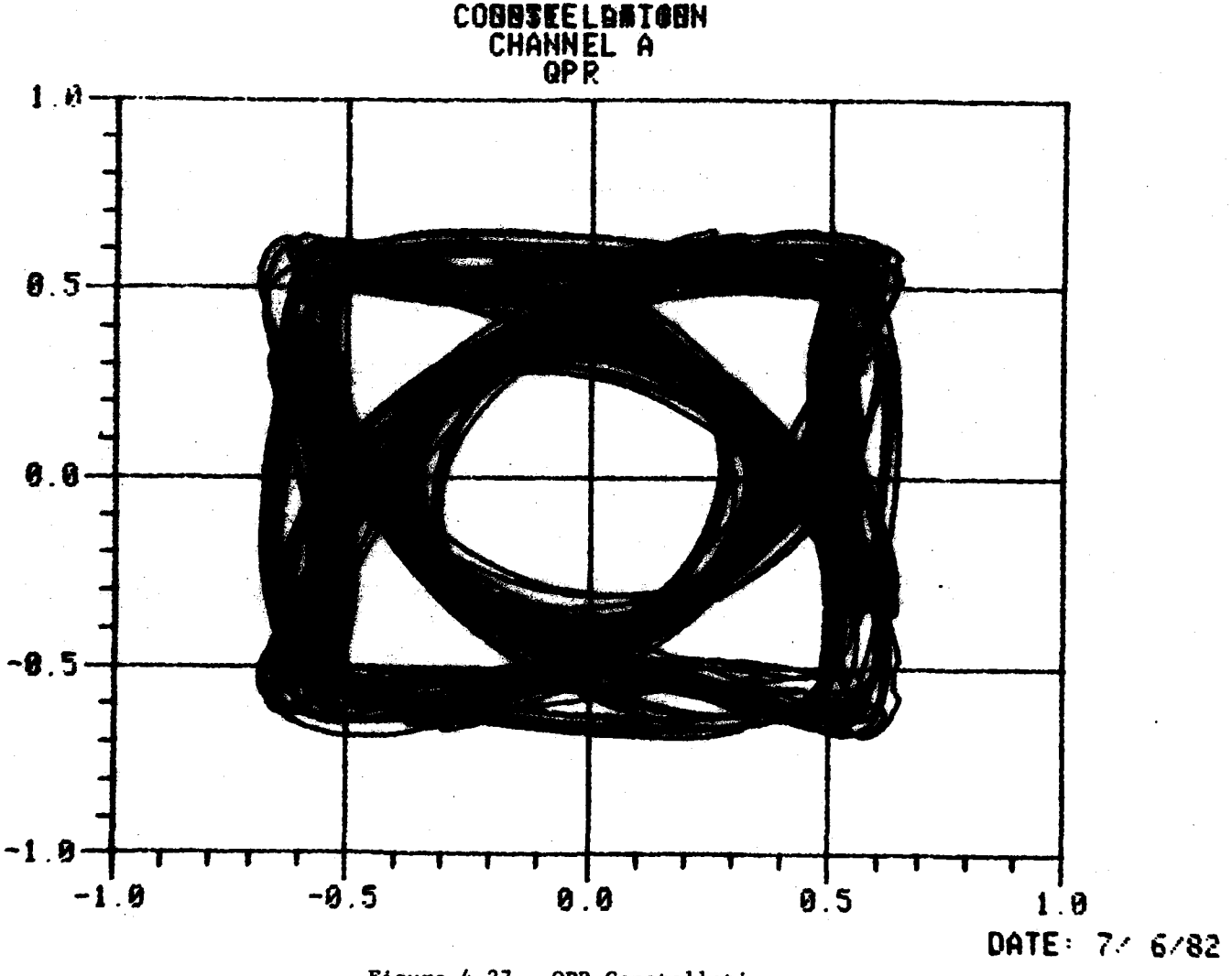


Figure 4-27. QPR Constellation

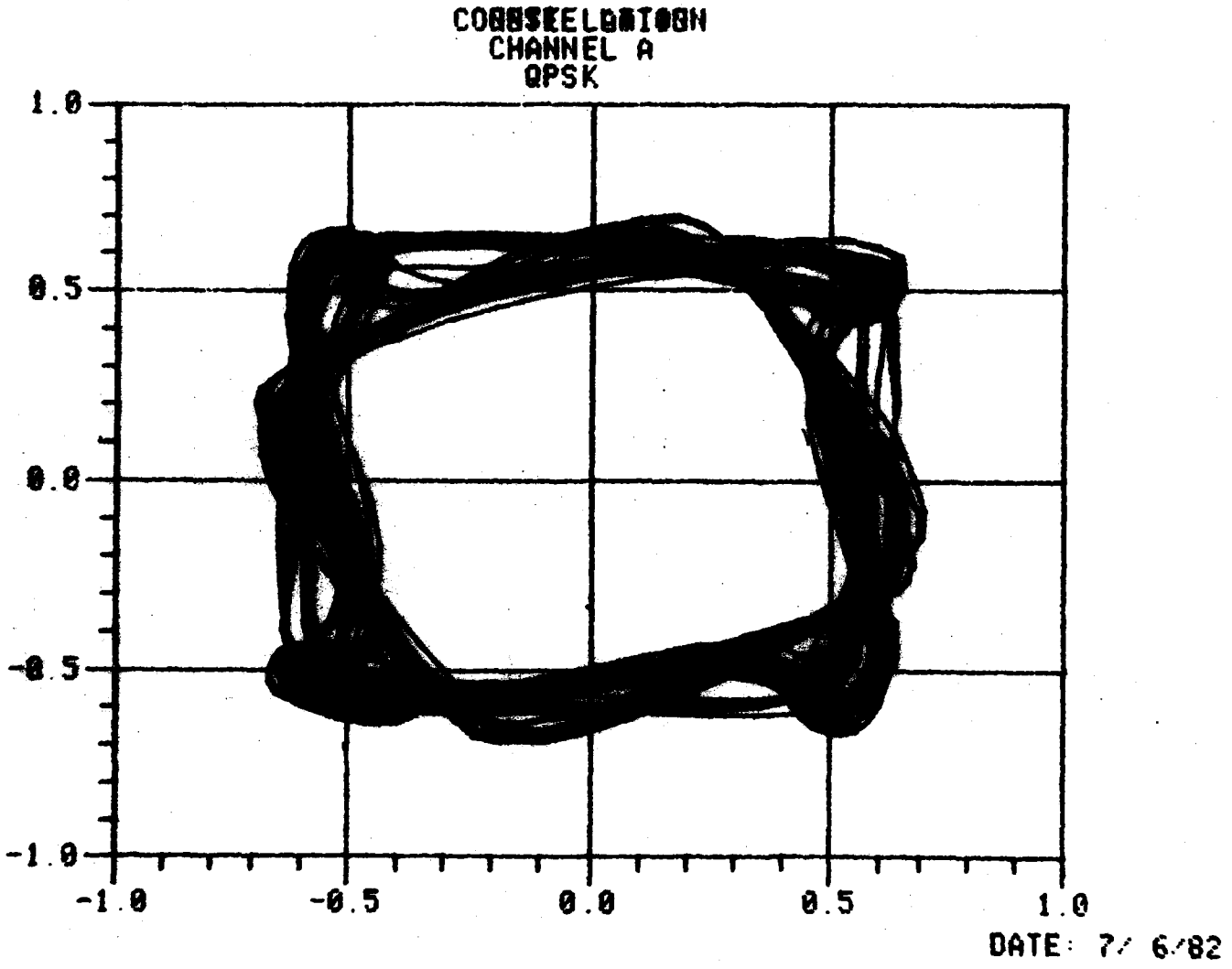


Figure 4-28. QPSK Constellation

The following is a list of the command mnemonics, their effect and any pertinent references for functions already described.

AGC — Used to control use of the AGC and its' bandwidth. (Section 4.5.6.1)

BITE — Controls bit error test. (Section 4.5.2)

CHN — Requests and sets the desired channel model. Note, fading channels only operative with execution of bit error test. (Section 4.5.6.1)

CRL — Sets the channel correlation coefficient.

```
...CRL
CHANNEL CORRELATION
COEFFICIENT  CF =.75
```

DPR — Requests and sets the drive power in dB. (Section 4.5.6.1)

DVR — Selects diversity function. If HYSTERESIS is selected, it then calls PEC for psuedo error counter register set-up.

```
DVR
 DIVERSITY TECHNIQUE
   1   AGC
   2   ISQM
   3   HYSTERESIS
   OPTION NO. =2
 DIVERSITY TECHNIQUE  ISQM
...PEC
 PSEUDO ERROR COUNTER

 REGISTER SIZE IN BITS =4
 FULL COUNT=   15
 ENTER INITIAL COUNTER VALUE  15


 ENTER INITIAL ON-LINE RECEIVER

 RECEIVER A/B 0/1  0
 PSEUDO ERROR COUNTER

 REGISTER SIZE IN BITS =    4
...
```

EBN — Requests and sets EB/NO for each channel (Section 4.5.6.1)

EYE — Plots the two baseband eye patterns for the requested (Section 4.5.7).

FLT — Sets an RF or IF filter to the type, order, bandwidth, and center frequency requested. (Section 4.5.5)

FRS — Takes and plots the frequency response of any of the available filters. (Section 4.5.4)

HELP — The word HELP is written out and the bell tone is sounded. This is repeated 5 times. Alternately, simultaneously depressing the CTRL key and H will produce the same result.

ITS — Sets the inter tap spacing for the channel model.

```
...ITS
INTER TAP SPACING
ITS = .8
```

LIS — Requests, takes, and plots a baseband constellation from the desired receiver (Section 4.5.8)

NLI — The transmitter non-linearity is put in or taken out. (Section 4.5.6.1)

OPTN — Brings in the OPTN dispatch system. (Section 4.5.1)

OTM — Sets the offset threshold monitor slicing level. (Section 4.5.6.1)

PEC — Sets the psuedo error counter register width, initial value and initial on-line receiver.

```
...PEC
PSEUDO ERROR COUNTER
REGISTER SIZE IN BITS =6
FULL COUNT=   63
ENTER INITIAL COUNTER VALUE  48
ENTER INITIAL ON-LINE RECEIVER
RECEIVER A/B 0/1  1
PSEUDO ERROR COUNTER

REGISTER SIZE IN BITS =    6
```

PSD — A PSD of the desired output is taken of the desired device and a plot of the data is given. (Section 4.5.3)

QPSK Sets the system modulation to QPSK. (Section 4.5.6.1)

QPR Sets the system modulation to QPR. (Section 4.5.6.1)

RF The transmitter RF filters may be put in or taken out. (Section 4.5.6.1)

RST Reinitializes the system processors by storing them in ROMSET, RC, and then clearing.

SCR The scrambler may be put in or taken out of the system. (Section 4.5.6.1)

TAP Removes and stores the current system frame pointer. (Section 4.5.6.1)

TESTAB [illegible]

TOURVB "TOURVB [illegible] produces a table of [illegible]

[illegible] (Section 3.1)

TSC [illegible]

CALIBRATION CURVE RESULTS

EB / N0	BER A	BER B	PER A	PER B
0.0	1.427E-01	1.577E-01	1.779E-01	1.866E-01
1.0	1.395E-01	1.463E-01	1.520E-01	1.433E-01
2.0	9.505E-02	1.027E-01	1.364E-01	1.393E-01
3.0	6.884E-02	7.047E-02	1.248E-01	1.141E-01
4.0	4.802E-02	5.162E-02	1.030E-01	1.010E-01
5.0	3.170E-02	3.040E-02	9.286E-02	7.309E-02
6.0	1.795E-02	1.836E-02	6.309E-02	5.720E-02
7.0	1.082E-02	9.036E-03	4.949E-02	4.041E-02
8.0	4.876E-03	5.257E-03	3.223E-02	2.670E-02
9.0	2.456E-03	1.684E-03	2.056E-02	1.670E-02
10.0	7.097E-04	9.355E-04	1.335E-02	1.026E-02
11.0	3.529E-04	2.647E-04	8.765E-03	5.765E-03
12.0	7.895E-05	5.263E-05	5.000E-03	2.421E-03
13.0	2.273E-05	0.000E+00	3.000E-03	1.091E-03

Figure 4-29. $CURVE Output

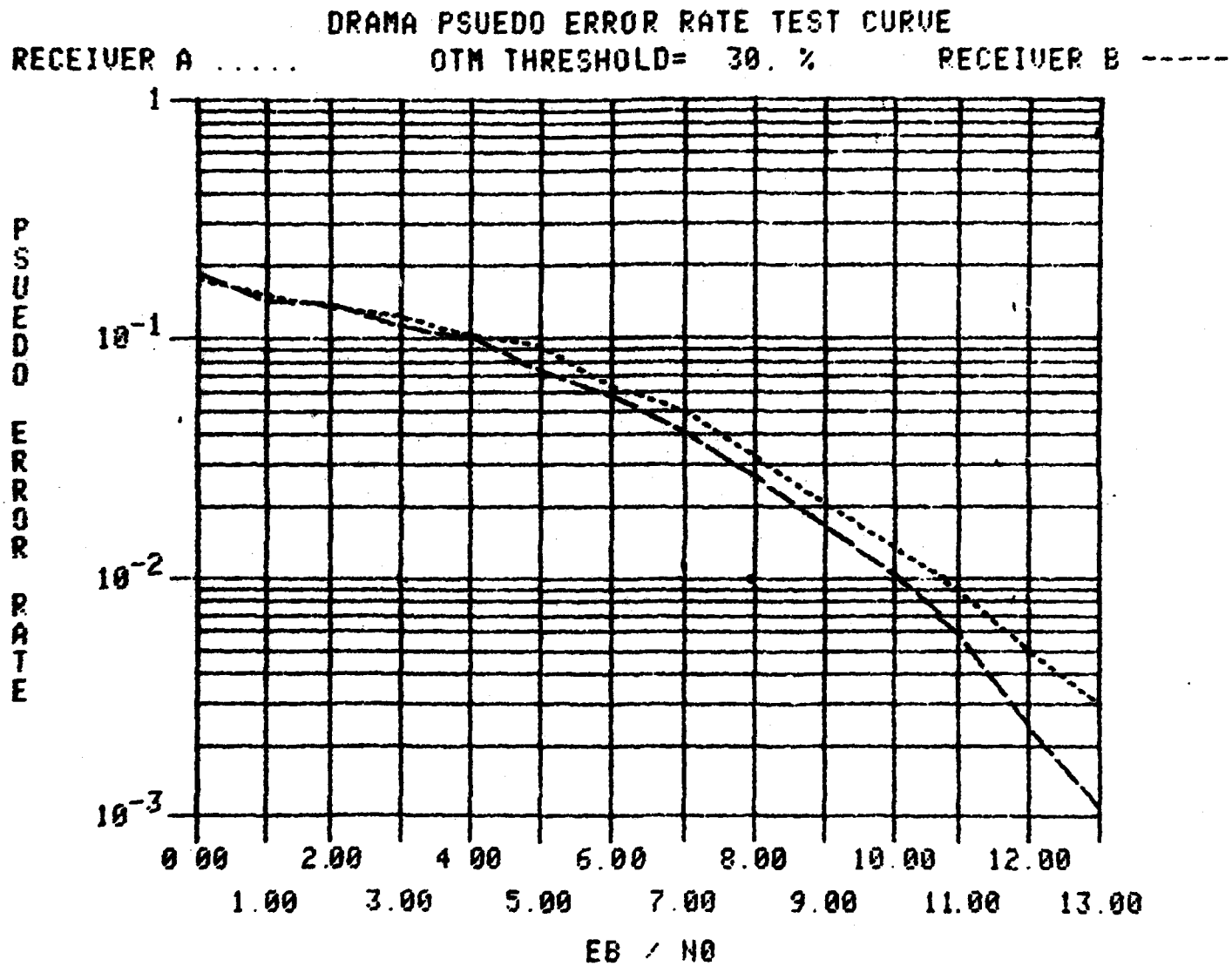


Figure 4-30. $CURVE Output

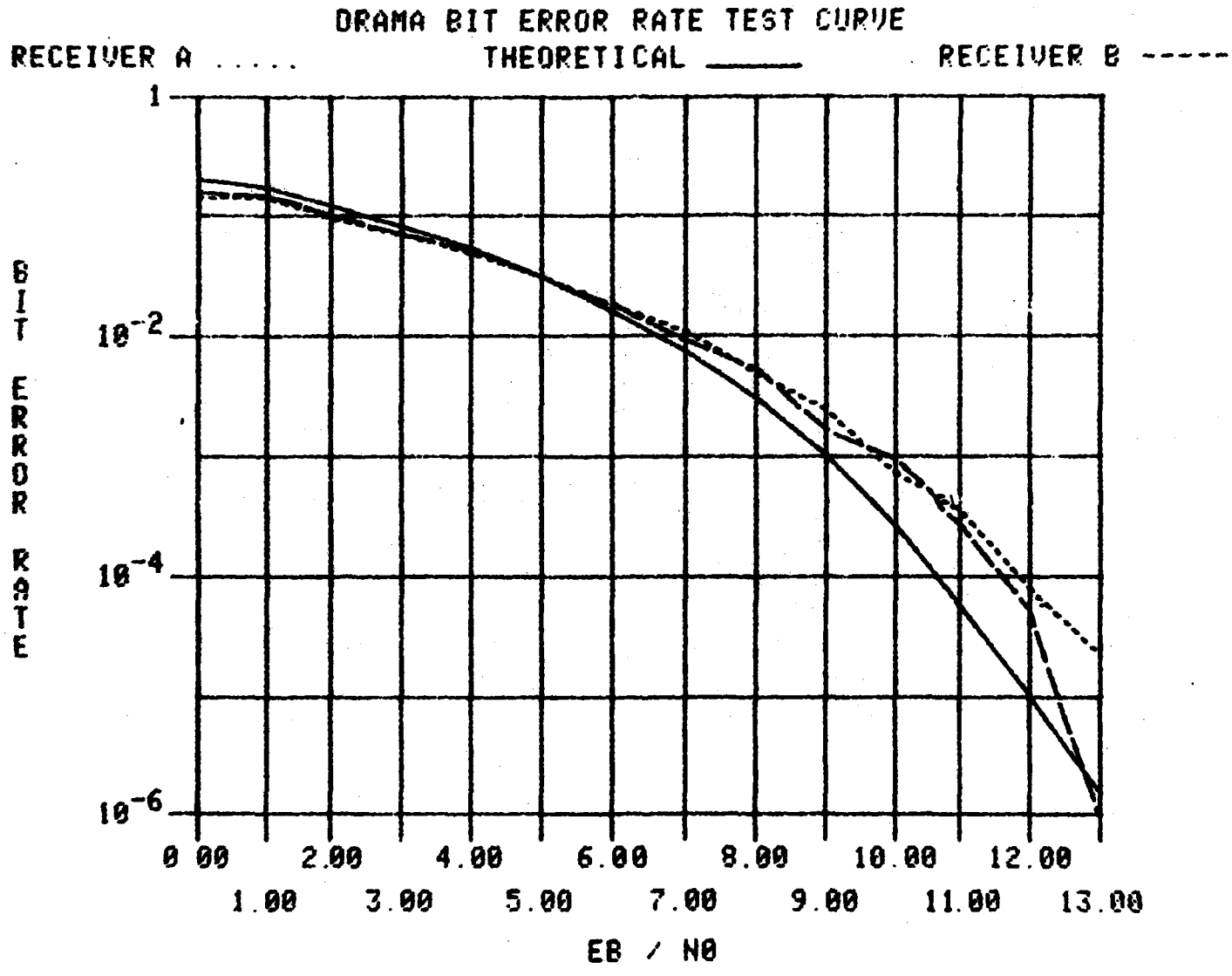


Figure 4-31. $CURVE Output

A typical set of eight simulation variables to the stripchart recorder are:

1 Logarithmic fading channel envelope, Receiver A

2 Logarithmic fading channel envelope, Receiver B

3 Bit errors, Receiver A

4 Bit errors, Receiver B

5 Bit errors, diversity

6 AGC amplitude, Receiver A

7 AGC amplitude, Receiver B

8 Status of diversity selector.

These simulation variables may be substituted for one or more of the above, such as the outputs of OTM for receivers A and/or B, or the coincidences between the diversity switch status and the RF envelope power.

Section 5 contains sets of typical stripplot outputs.

5.0 SYSTEM VERIFICATION AND TEST RESULTS

The DRAMA AN/FRC-170(V) radio simulation has been used extensively by engineers at DCEC to both verify its' various areas of performance in known cases and to gather data in a purely experimental mode for design criteria proposals.

Some of the runs performed by engineers at DCEC through the remote terminal links, have been used for the purposes described below.

An extensive study into the area of diversity error minimization was made by means of psuedo error counter width adjustment. The test results showed a minimum error count by use of a 4 to 5 bit counter.

Pseudo error count as a function of pseudo error window width was also tested by DCEC engineers. Window widths of 20%, 25%, and 30% produces results in close agreement to theoretical expectations.

Upon completion of the pseudo error window width study, an examination of the relationship between pseudo error rate and bit error rate was undertaken. Theoretical conclusions showed a linear relationship between the two. Extensive testing with the hybrid simulation bore out the expected result. This conclusion allows the modem user a way of estimating actual bit error rate by knowing only pseudo error rate, which is easily measurable.

5.1 Automatic Bit Error Rate, Psuedo Error Rate Plotting

As part of the task 4 in the contractual statement of work, R220-81-011, the Engineering Computing Center at Martin Marietta was to provide the capability to plot a continuous graph of actual bit error rate versus EB/NO, derived from runs made on the hybrid simulation. Also plotted on the graph is a theoretical curve of the same information.

For QPR, an additional plot of psuedo error rate versus EB/No and a tabular listing of the plotted results are supplied. Figures 5-1 through 5-4 are typical sets of output for QPSK and QPR respectively.

5.2 Stripplot Outputs

The hybrid simulation presently has the capability to transmit eight multiplexed channels of analog data over a phone link to DCEC. Some typical plots of these analog data are included in this section. In addition to the stripplot there are many pertinent digital input and output data associated with each run.

Figure 5-5 is a listing of the digital control set-up input and resultant output of a run tailored to exhibit the ISQM operation.

The psuedo error counter was set to a small value of only 3 bits to generate sufficient switching for demonstrative purposes. An EB/NO of 10 dB was used with no channel fading.

Figure 5-6 is an analog stripplot set of the run. Insepction of the diversity error trace reveals proper switching between receivers A and B.

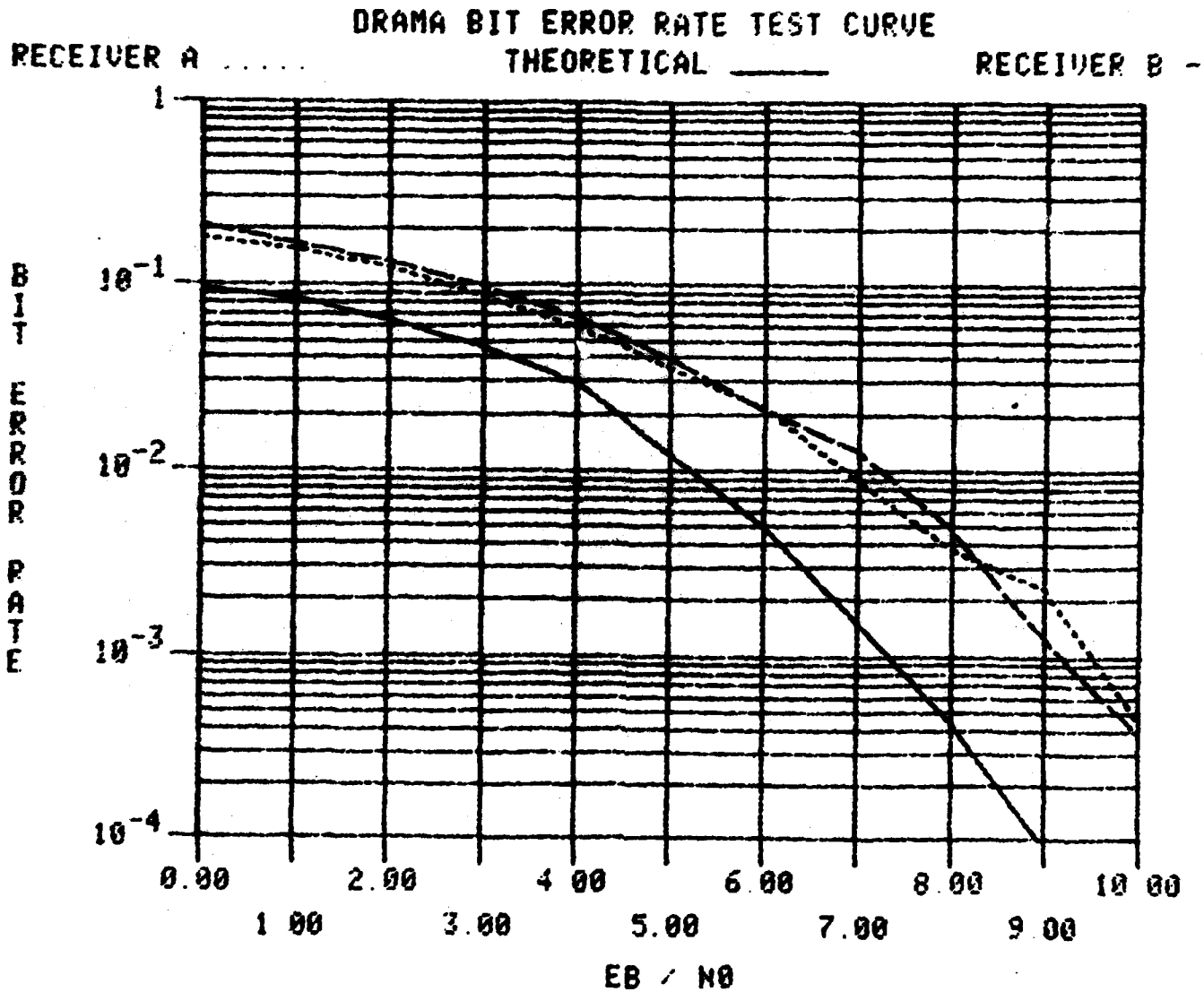


Figure 5-1. QPSK BER vs. EB/NO Plot

CALIBRATION CURVE RESULTS

EB / N0	BER A	BER B	PER A	PER B
0.0	1.615E-01	1.839E-01	1.844E-01	1.986E-01
1.0	1.612E-01	1.740E-01	1.573E-01	1.497E-01
2.0	1.100E-01	1.139E-01	1.475E-01	1.543E-01
3.0	7.815E-02	9.096E-02	1.254E-01	1.414E-01
4.0	5.773E-02	6.062E-02	1.106E-01	1.158E-01
5.0	3.934E-02	3.959E-02	9.286E-02	9.156E-02
6.0	2.688E-02	2.507E-02	7.243E-02	7.397E-02
7.0	1.476E-02	1.484E-02	5.455E-02	5.505E-02
8.0	7.429E-03	7.352E-03	3.680E-02	3.950E-02
9.0	3.474E-03	2.982E-03	2.582E-02	2.519E-02
10.0	9.677E-04	1.290E-03	1.632E-02	1.516E-02
11.0	4.118E-04	5.000E-04	8.706E-03	8.824E-03
12.0	2.368E-04	1.316E-04	5.000E-03	5.421E-03
13.0	6.818E-05	6.818E-05	2.136E-03	2.818E-03

Figure 5-2. QPR Tabular Result

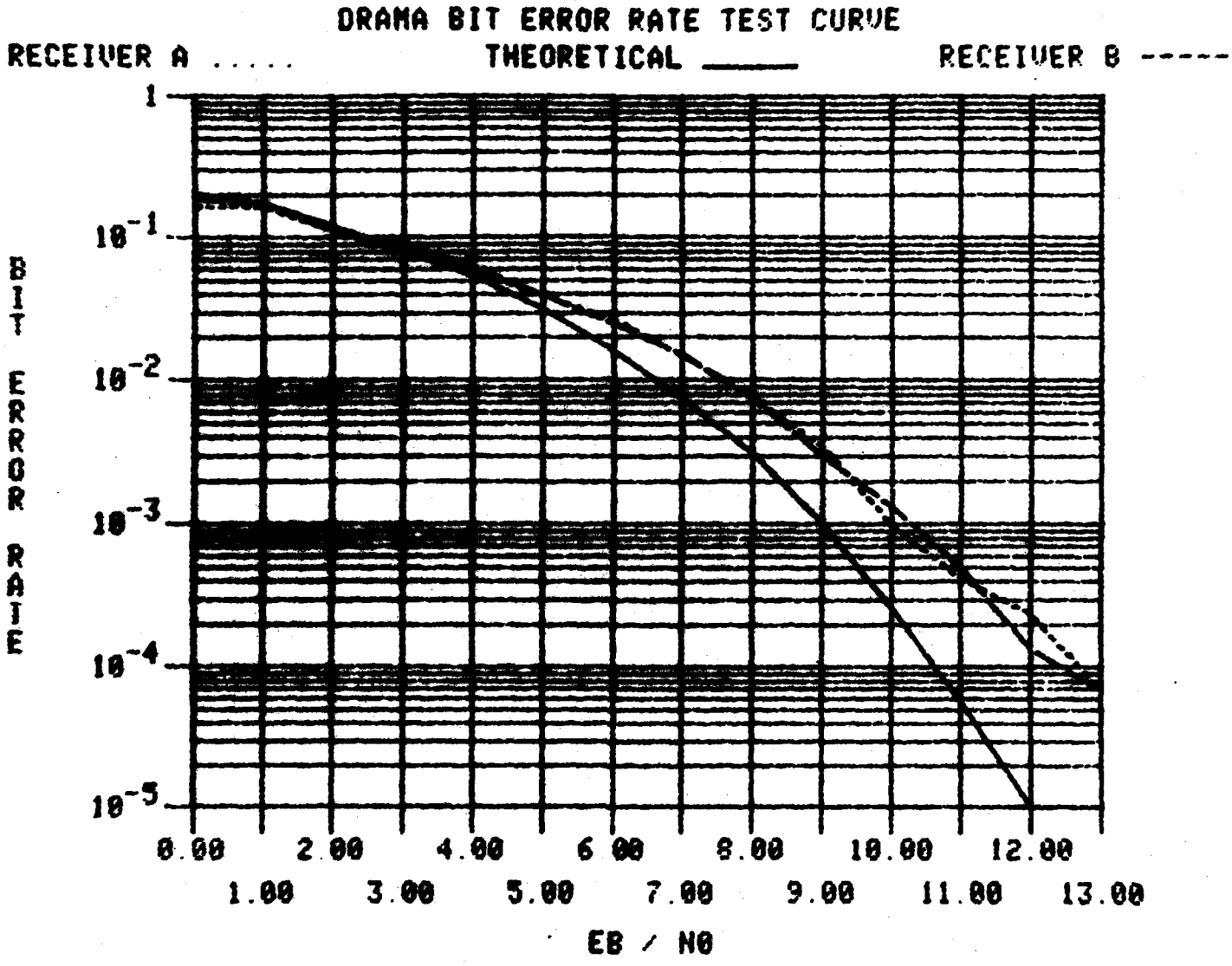


Figure 5-3. QPR BER vs. EB/NO Plot

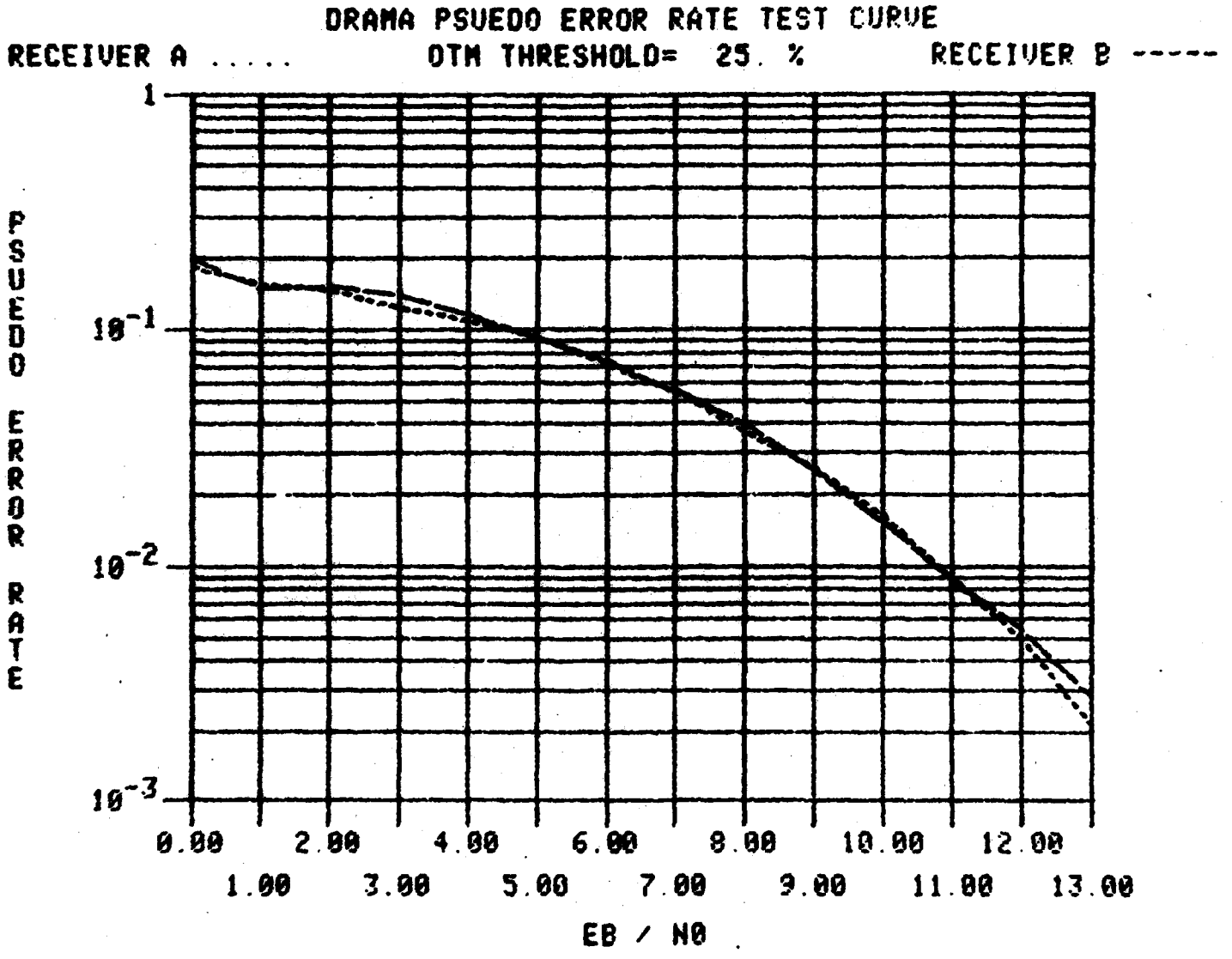


Figure 5-4. QPR PER vs. EB/NO Plot

```
DVR
 DIVERSITY TECHNIQUE
   1    AGC
   2    ISQM
   3    HYSTERESIS
   OPTION NO. =2
 DIVERSITY TECHNIQUE  ISQM
  PEC
 PSEUDO ERROR COUNTER

 REGISTER SIZE IN BITS =3
 FULL COUNT=    7
 ENTER INITIAL COUNTER VALUE  3


 ENTER INITIAL ON-LINE RECEIVER

 RECEIVER A/B 0/1  0
 PSEUDO ERROR COUNTER

 REGISTER SIZE IN BITS =    3
  BITE
 CHANNEL MODEL ?
   1    OUT
   2    RAYLEIGH
   3    LOS
        OPTION NO. =1
ENTER EB/N0 FOR CHANNEL A
10
ENTER EB/N0 FOR CHANNEL B
10
 RUN TIME =40

 BIT ERROR TEST IN PROGRESS
 PRESS <RETURN> FOR EARLY TERMINATION
```

```
TOTAL RUN TIME =   40.000  SECONDS
TOTAL BITS =     40000

                BIT ERRORS      BER

CHANNEL A          121     3.025E-03
CHANNEL B           54     1.350E-03
DIVERSITY          107     2.675E-03

PSEUDO ERROR COUNTERS

CHANNEL A COUNT=          404
CHANNEL B COUNT=          722
```

Figure 5-5. Digital I/O For Figure 5-6 Run

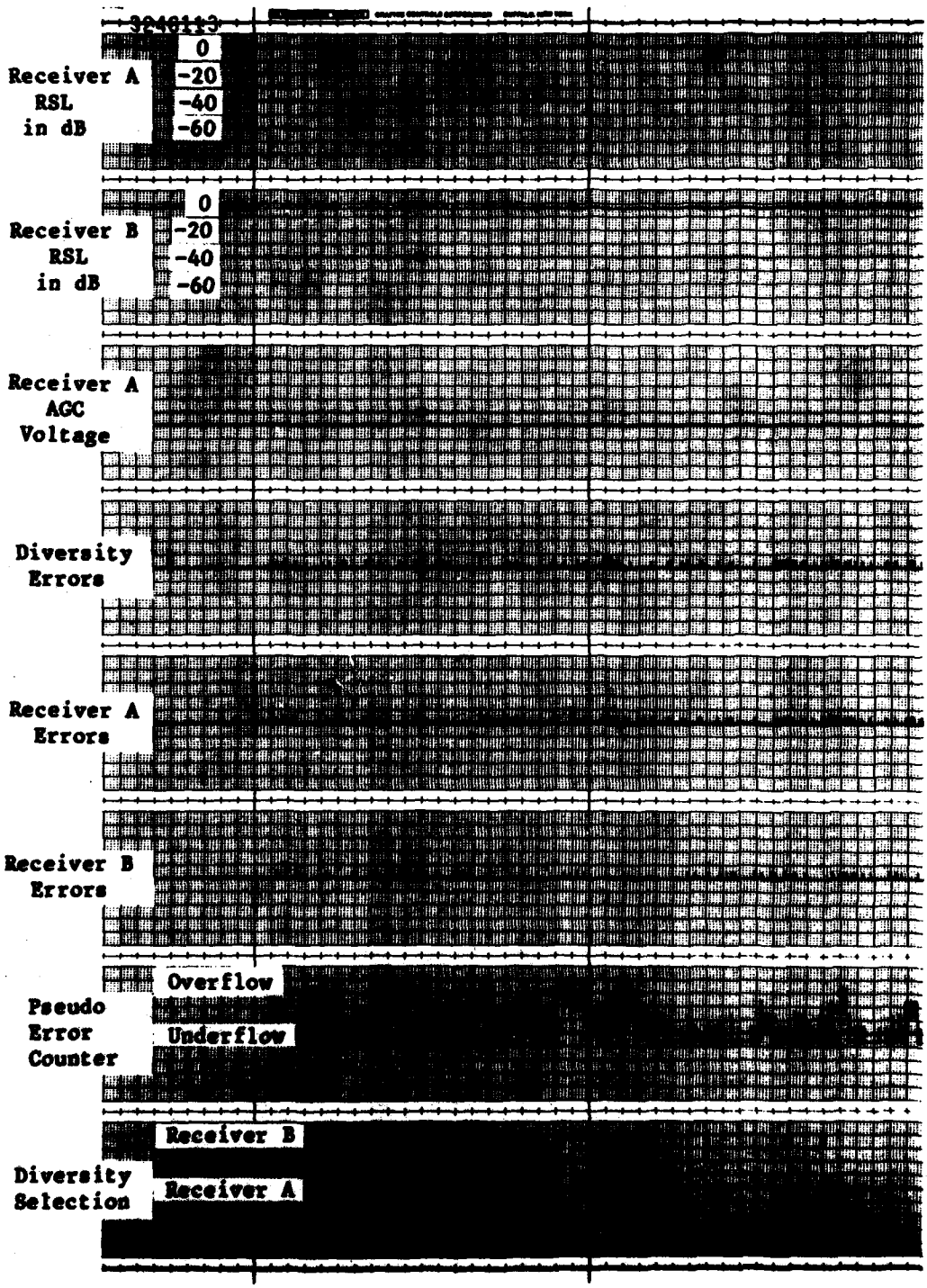


Figure 5-6. Analog Plot of ISQM Study

Figure 5-7 is a set of analog data associated with a study of ISQM diversity switch over time as a function of psuedo error counter register length. 10 dB of EB/NO was used throughout the 5 runs with PEC register lengths ranging from 2 to 6 bits in width.

The next run is of the HYSTERESIS study type. The HYSTERESIS run is used to optimize time and accuracy in the study of excess errors and false switching errors. Instead of making several individual runs, each of which requires approximately 30 seconds of overhead time in data entry and system initialization, a single set of data is entered, the system is initialized and any number of runs can be made and averaged.

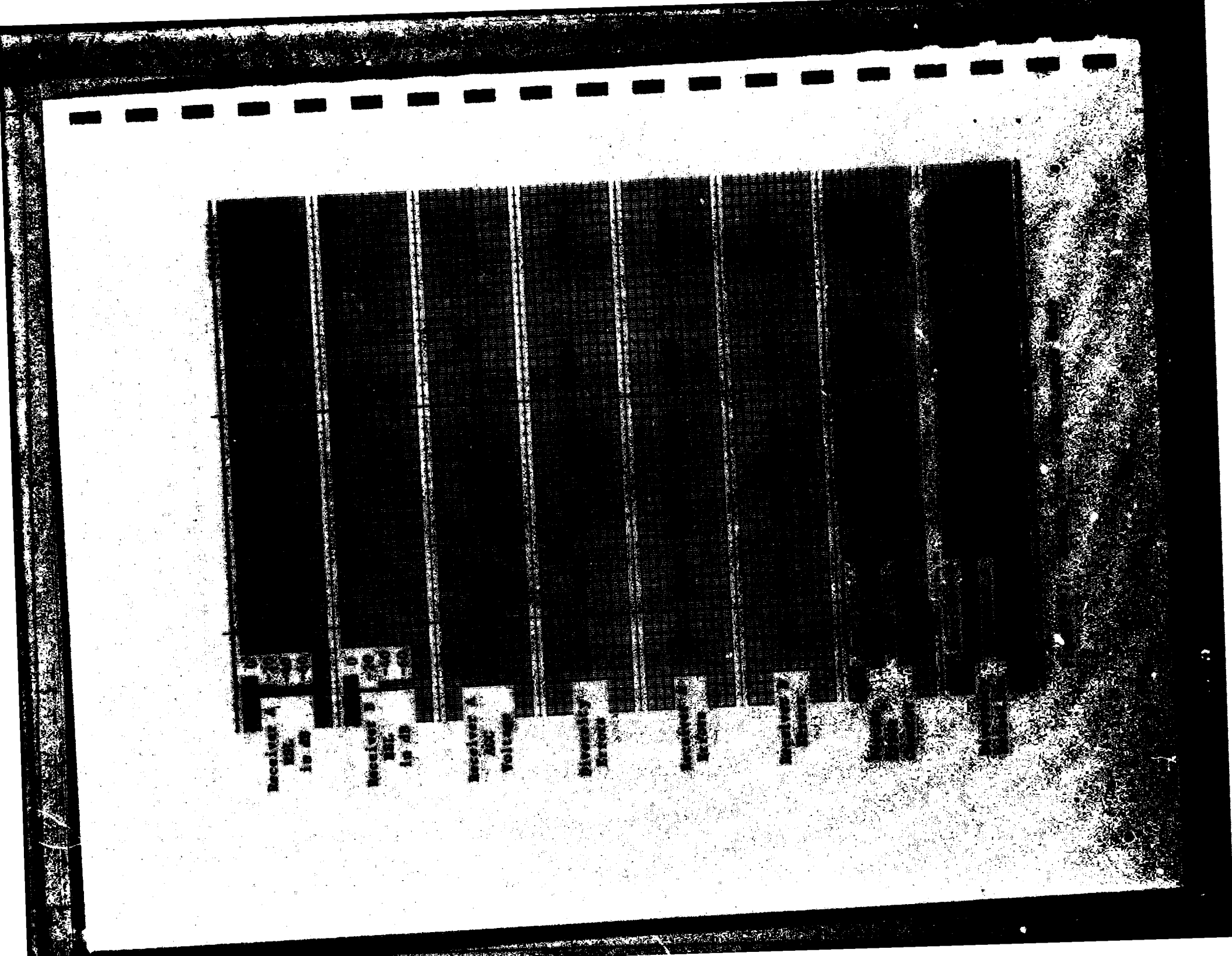
The digital entry for this technique is depicted in Figure 5-8 along with the averaged run results. Figure 5-9 is the analog stripplot of the result.

In this case, 10 runs were averaged. After a diversity switch due to the higher noise level in Channel B, the PEC register and diversity selection are reinitialized and the run sequence continues.

Figure 5-10 is a listing of digital input controlling the following run, and the resulting output after completion.

The run was with a Rayleigh fading channel with a fade cut-off characteristic of 0.01 Hz. The RSL diversity selection was used. The AGC was set at 0.5 Hz.

A high signal to noise ratio was used to allow bit error study at deep fade outages.



```
DVR
 DIVERSITY TECHNIQUE
   1    AGC
   2    ISQM
   3    HYSTERESIS
   OPTION NO. =3
 PSEUDO ERROR COUNTER

 REGISTER SIZE IN BITS =5
 FULL COUNT=   31
 ENTER INITIAL COUNTER VALUE  31


 ENTER INITIAL ON-LINE RECEIVER

 RECEIVER A/B 0/1  1

 HOW MANY RUNS?
10
 DIVERSITY TECHNIQUE  HYSTERESIS
...BITE
 CHANNEL MODEL ?
   1    OUT
   2    RAYLEIGH
   3    LOS
        OPTION NO. =1
ENTER EB/N0 FOR CHANNEL A
10
ENTER EB/N0 FOR CHANNEL B
8
 RUN TIME =100

 BIT ERROR TEST IN PROGRESS
 PRESS <RETURN> FOR EARLY TERMINATION
```

```
TOTAL RUN TIME =    0 977  SECONDS
TOTAL BITS =        976

                BIT ERRORS      BER

CHANNEL A           1     1.633E-03
CHANNEL B           6     7.065E-03
DIVERSITY           6     7.065E-03

PSEUDO ERROR COUNTERS

CHANNEL A COUNT=          11
CHANNEL B COUNT=          44


NUMBER OF RUNS AVERAGED =    10
...
```

Figure 5-8. HYSTERESIS Digital I/O

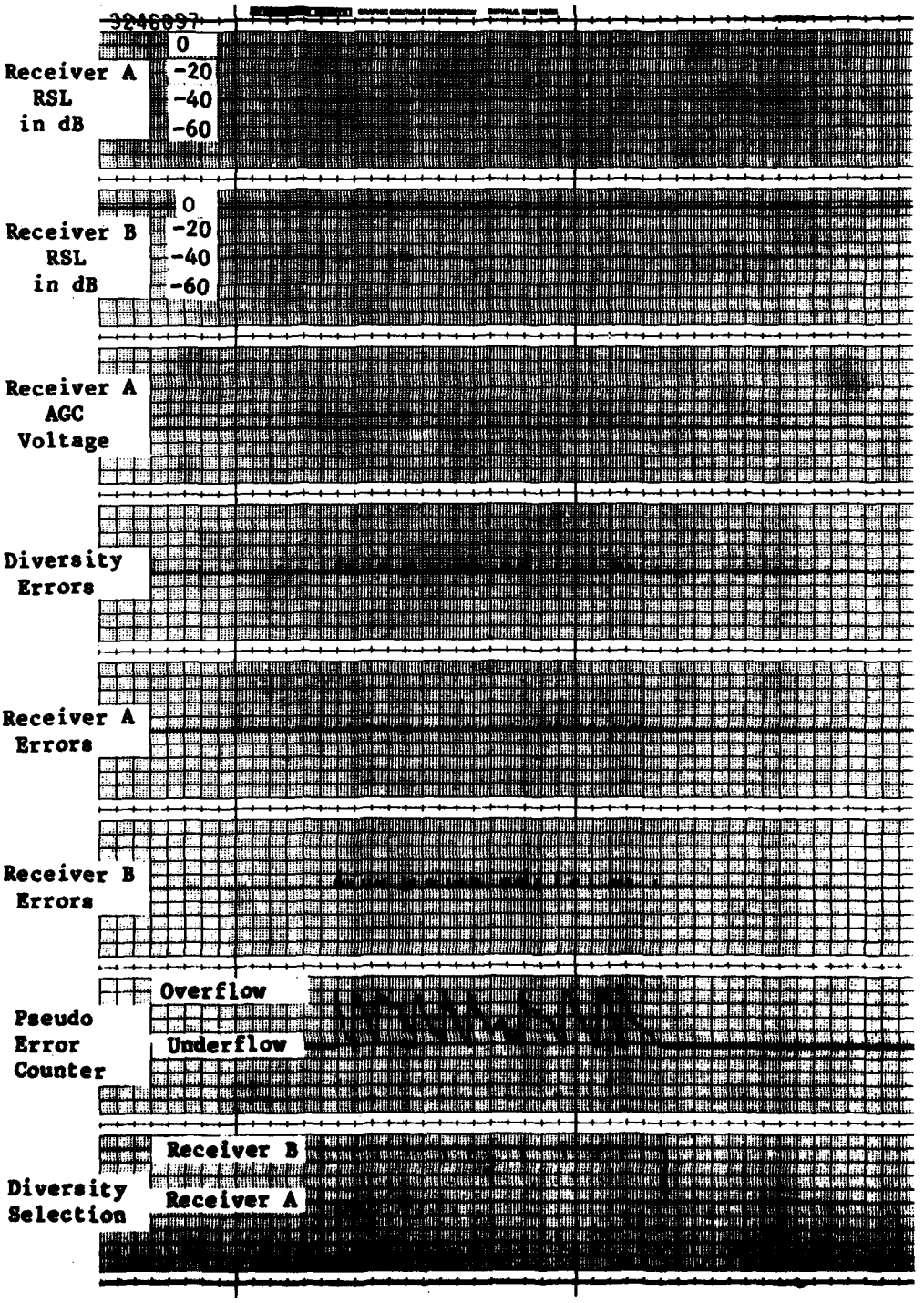


Figure 5-9. Analog Plot of HYSTERESIS Study

```
  .BITE
 CHANNEL MODEL ?
   1    OUT
   2    RAYLEIGH
   3    LOS
        OPTION NO. =2
ENTER FADE RATE IN HZ FOR CHANNEL A
0.<REAL<=1.
 .01
ENTER FADE RATE IN HZ FOR CHANNEL B
0.<REAL<=1.
 .01
ENTER EB/N0 FOR CHANNEL A
100
ENTER EB/N0 FOR CHANNEL B
100
 RUN TIME =400

 BIT ERROR TEST IN PROGRESS
 PRESS <RETURN> FOR EARLY TERMINATION


 TOTAL RUN TIME =  400.000  SECONDS
 TOTAL BITS =    400000

              BIT ERRORS      BER

 CHANNEL A        180     4.500E-04
 CHANNEL B         25     6.250E-05
 DIVERSITY          0     0.000E+00

 PSEUDO ERROR COUNTERS

 CHANNEL A COUNT=         237
 CHANNEL B COUNT=          76
```

Figure 5-10. Digital I/O For Rayleigh Channel Run

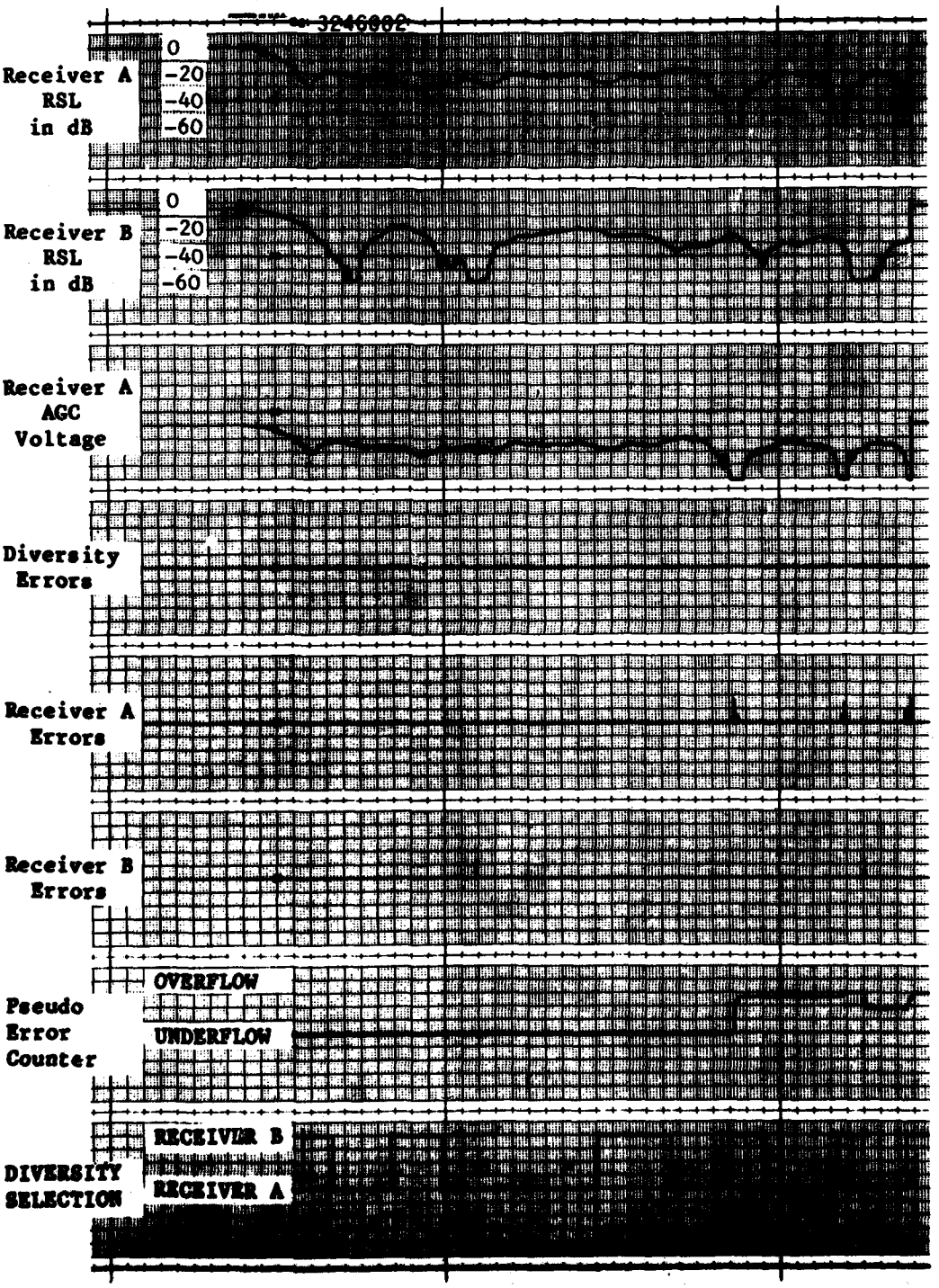


Figure 5-11. Analog Plot of Rayleigh Channel Run

As can be seen from the listing of Figure 5-10, bit error rates of approximately 10^{-5} accrued due to fade outages alone.

The nominal value of 6 dB was used as the RSL diversity switch over point. Analog stripplots were recorded during the run (see Figure 5-11) to exhibit the diversity switching characteristics.

5.3 Frequency Responses and Power Spectral Densities

As part of the daily system checkout and calibration routine, all of the IF, RF, and baseband filters have frequency response checks run on them. A PSD is performed on the modulator output for QPSK and QPR.

Figures 5-12 through 5-25 are a typical set of these results.

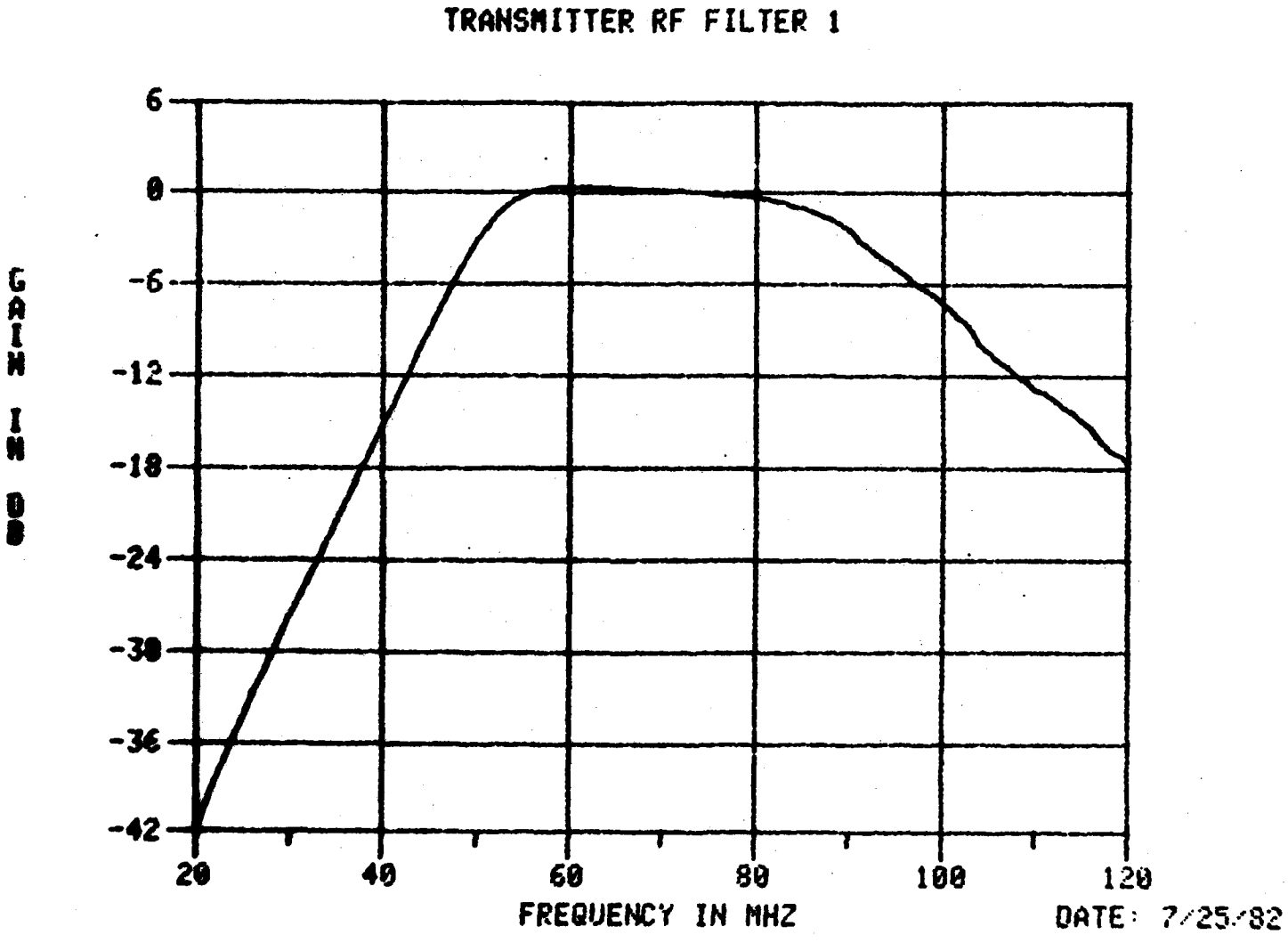


Figure 5-12. Calibration Plot

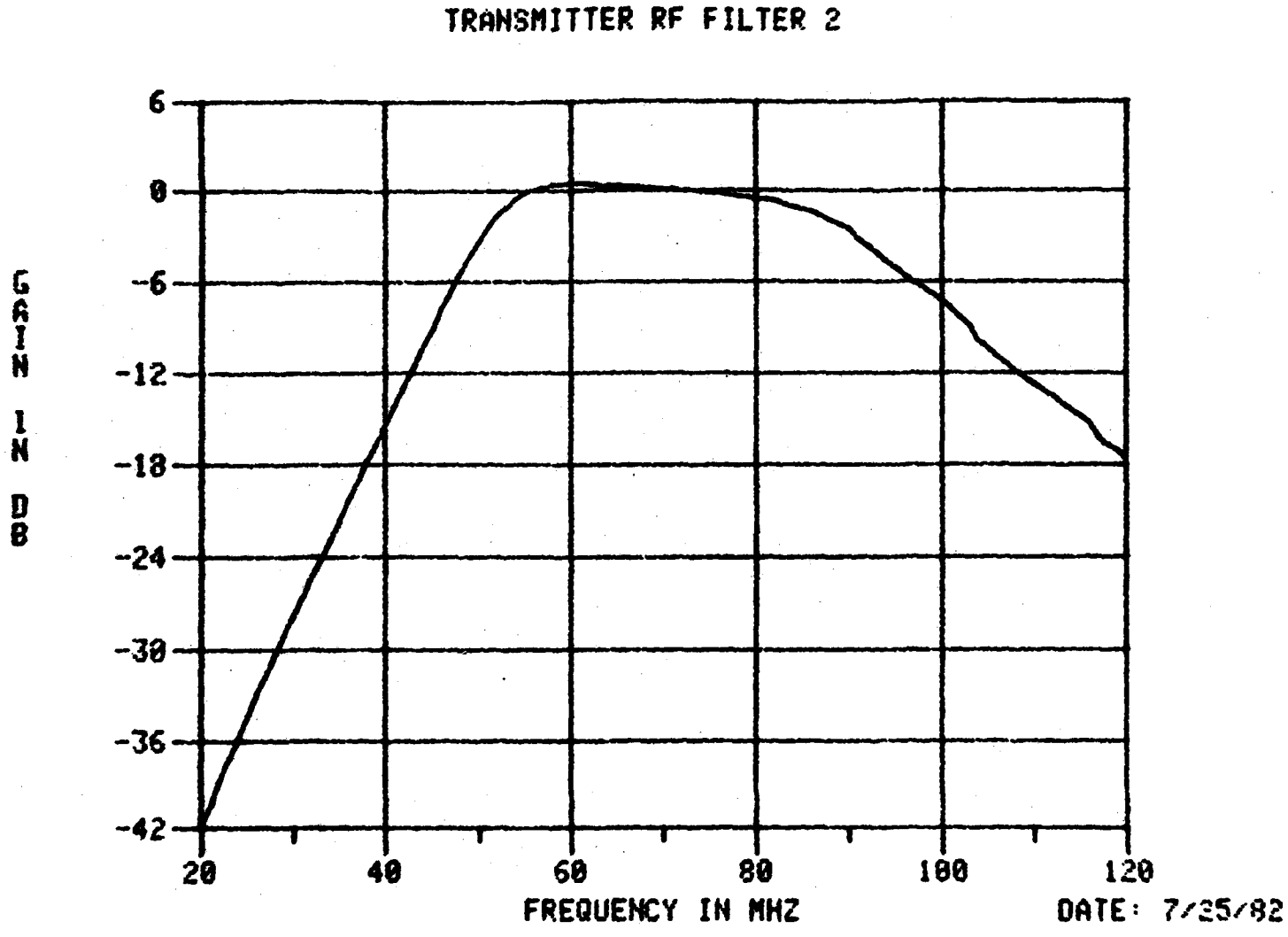


Figure 5-13. Calibration Plot

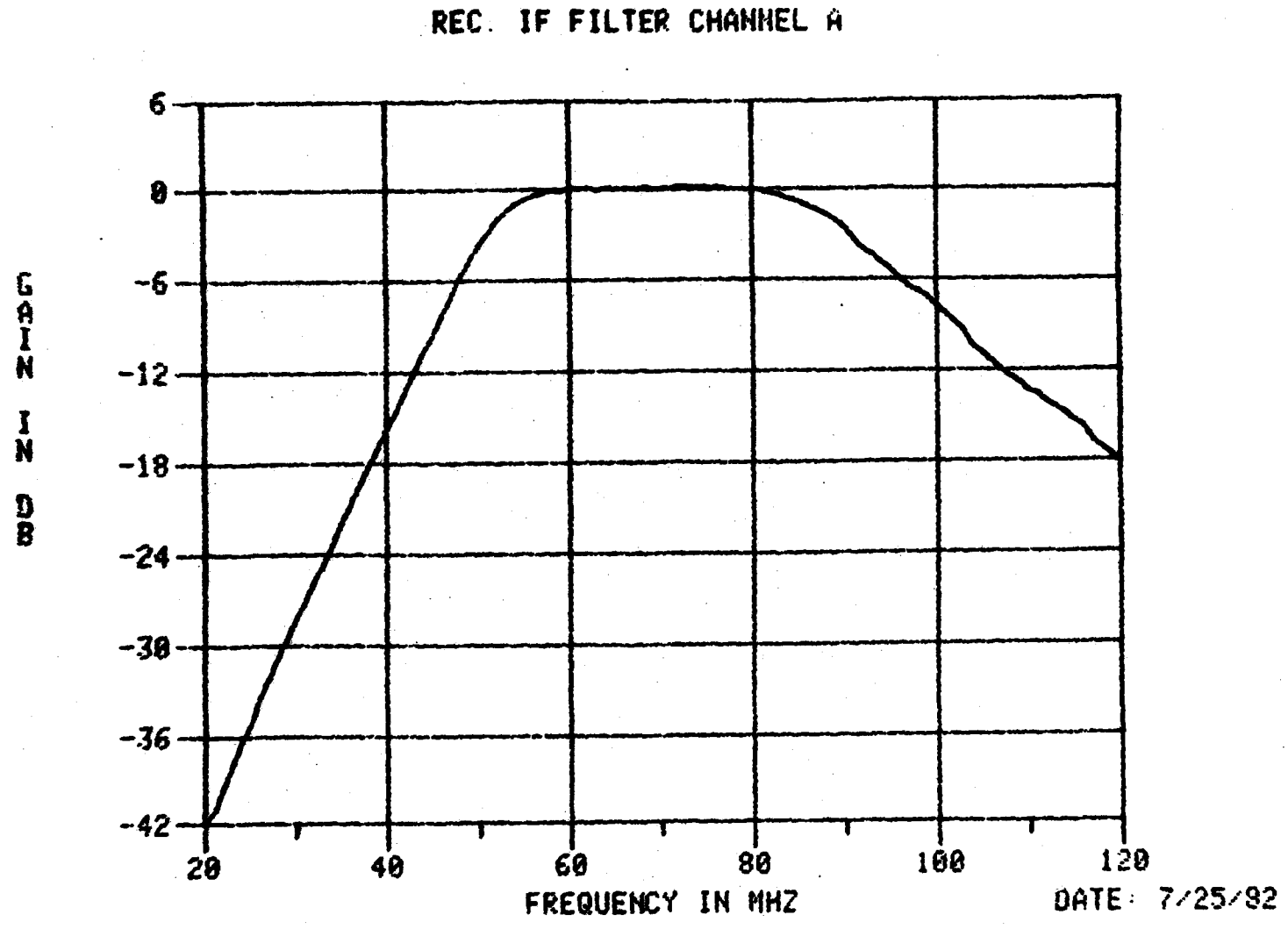


Figure 5-14. Calibration Plot

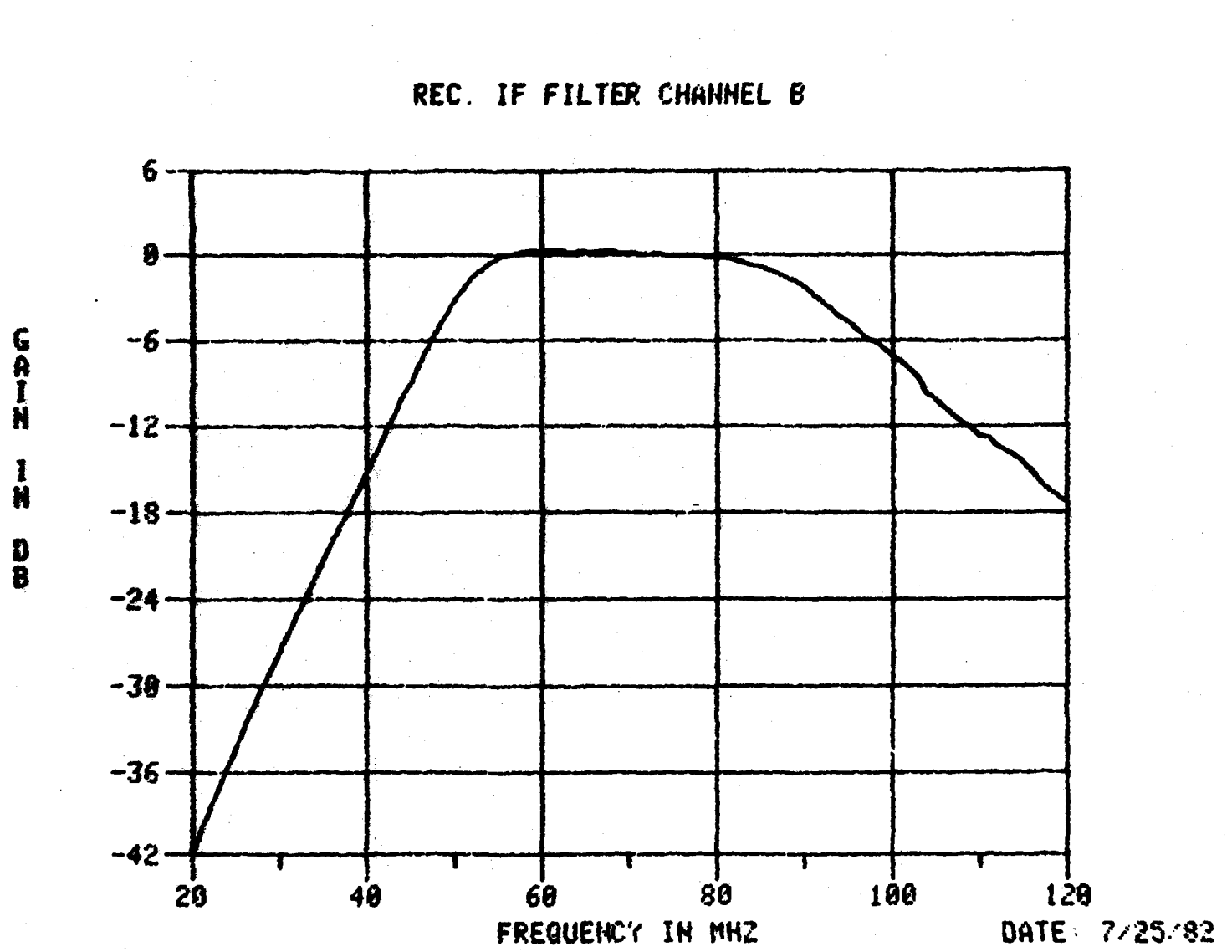
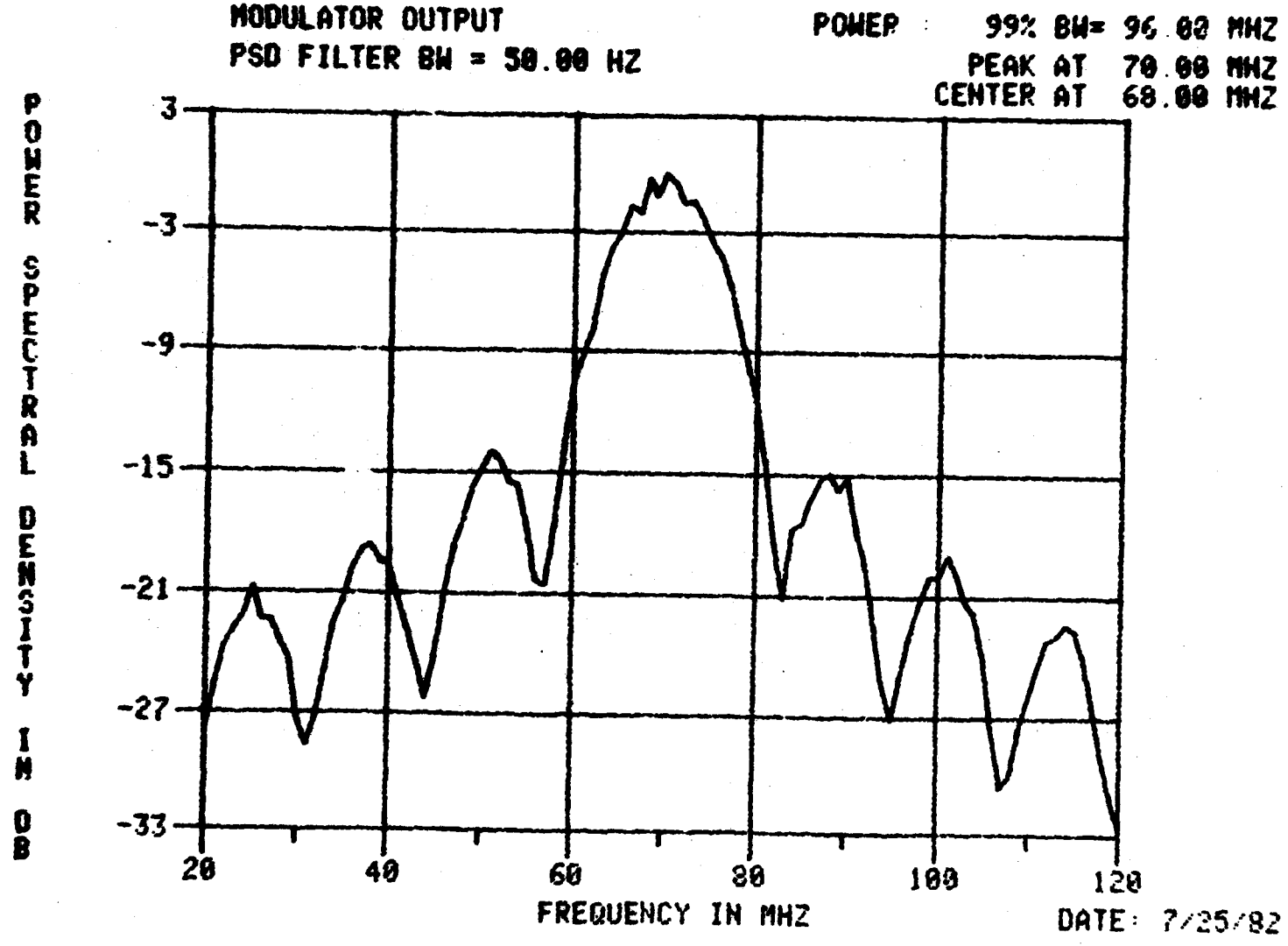


Figure 5-15. Calibration Plot



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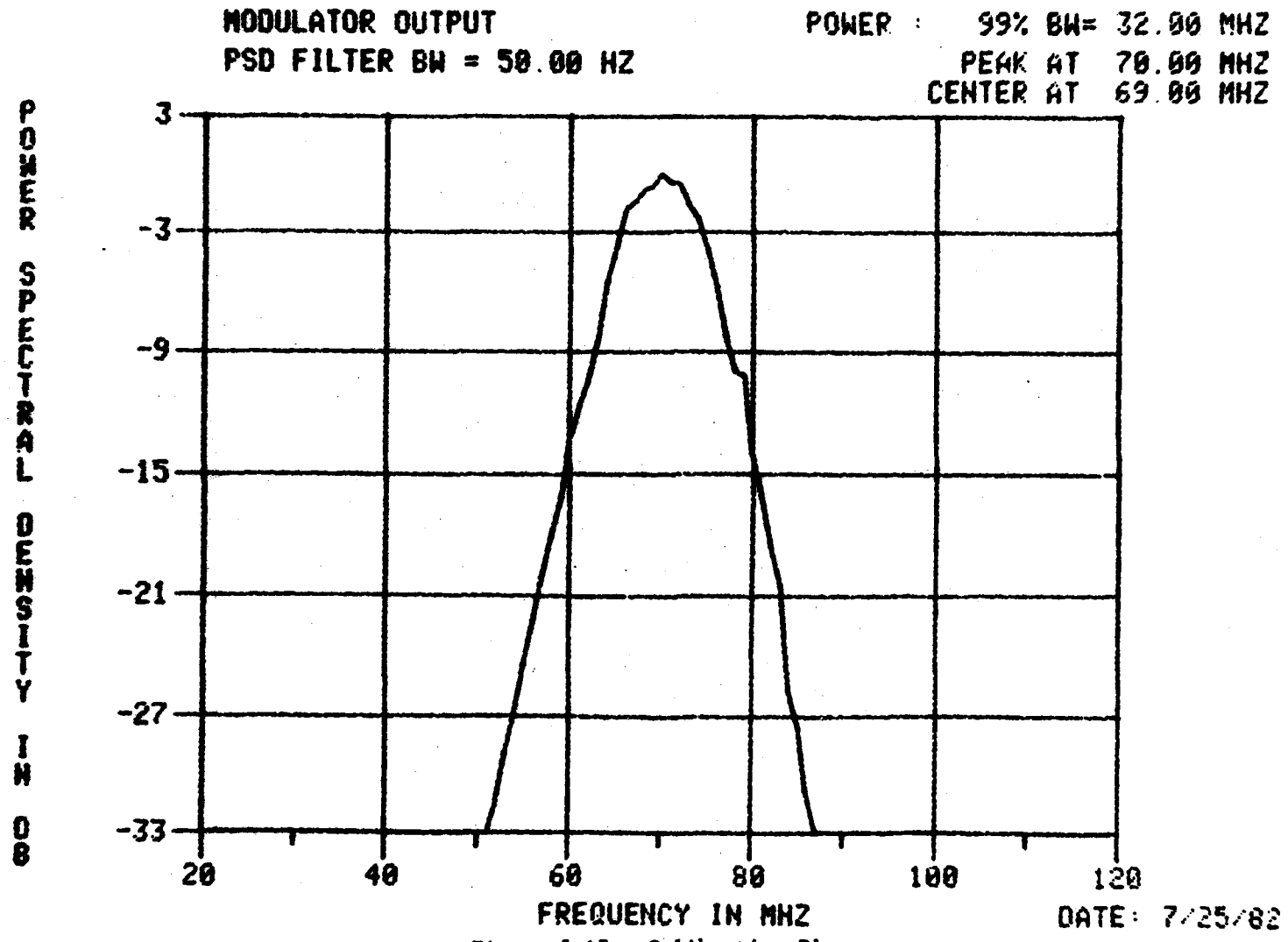

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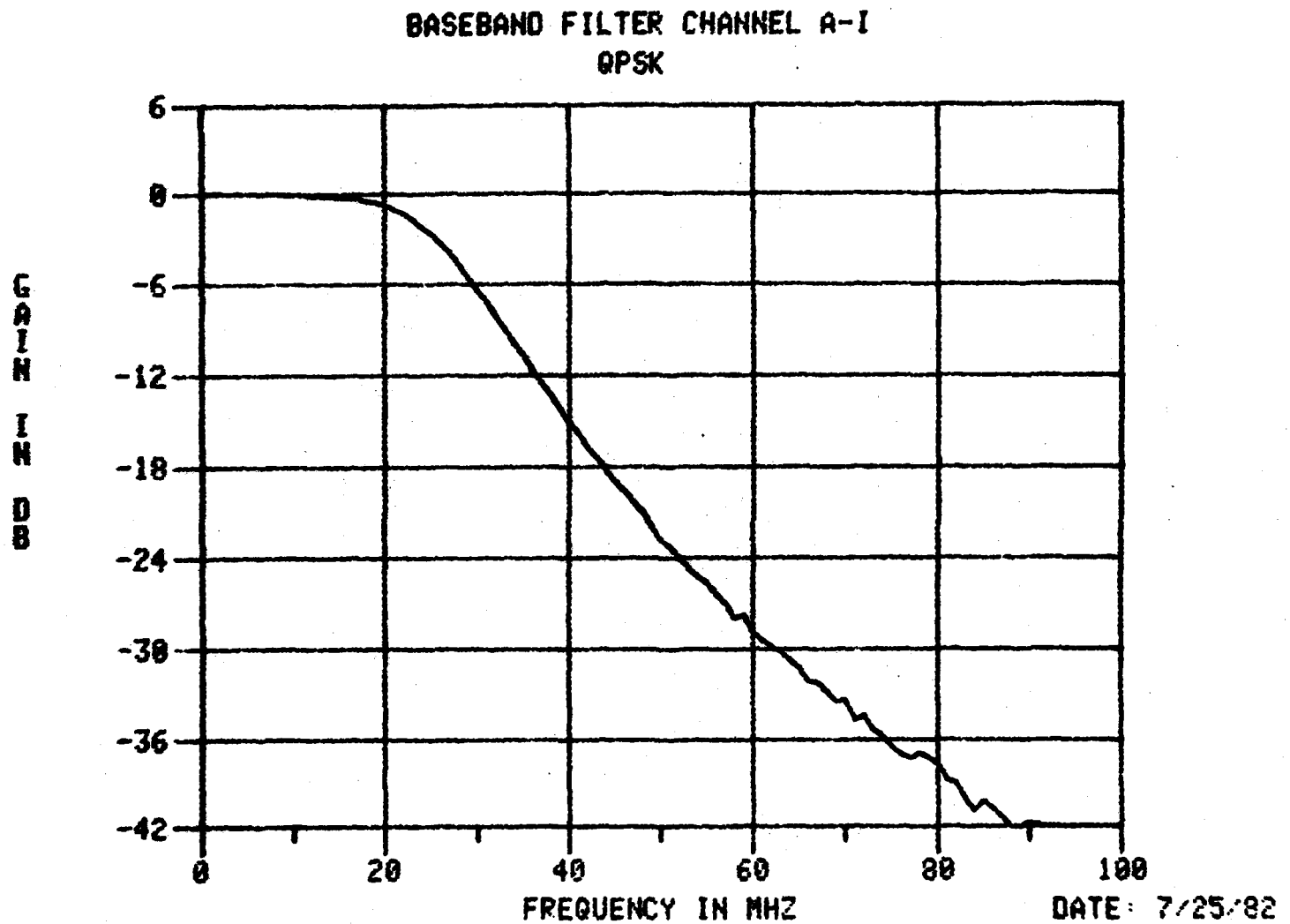

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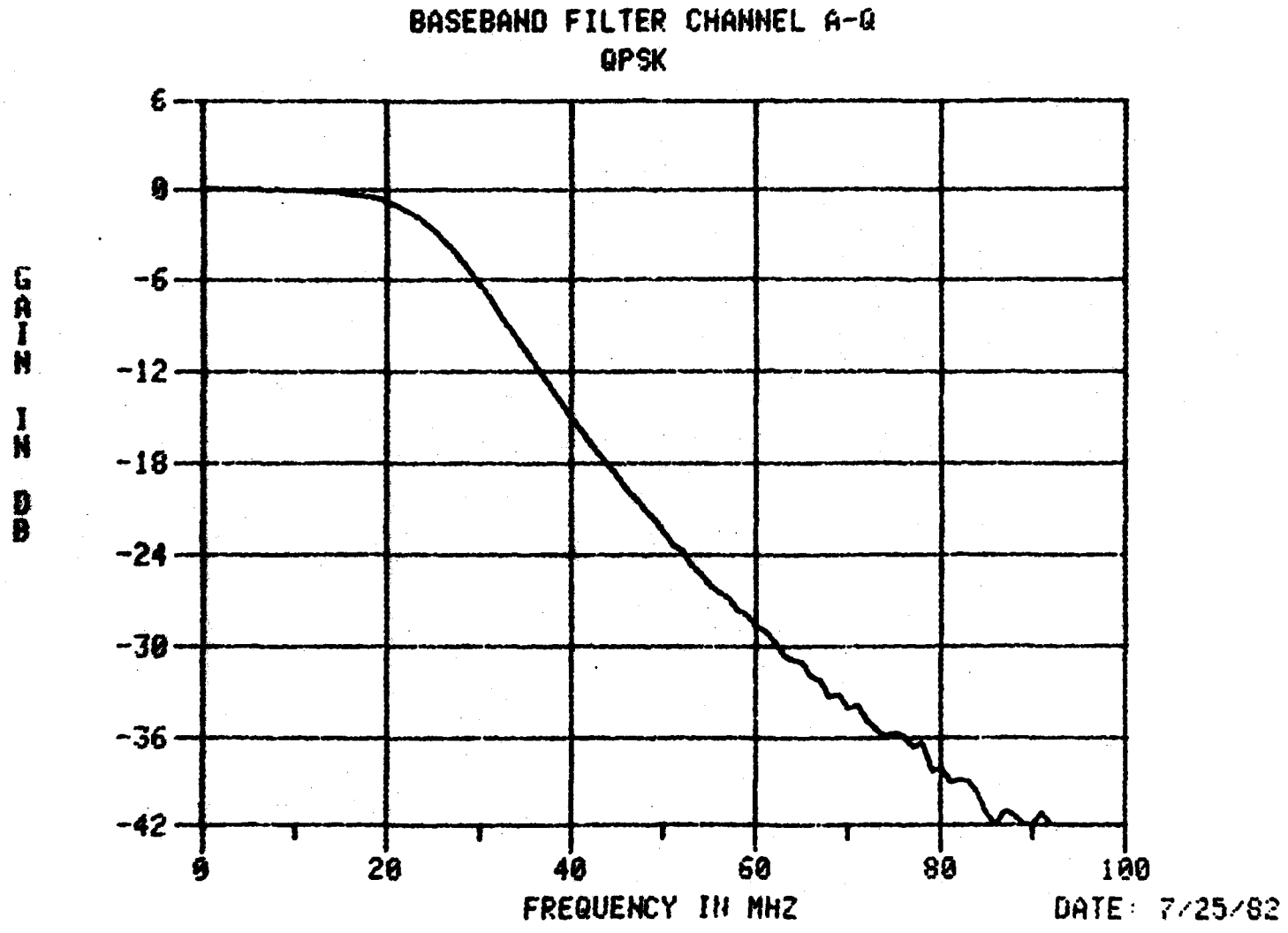

Figure 5-19. Calibration Plot

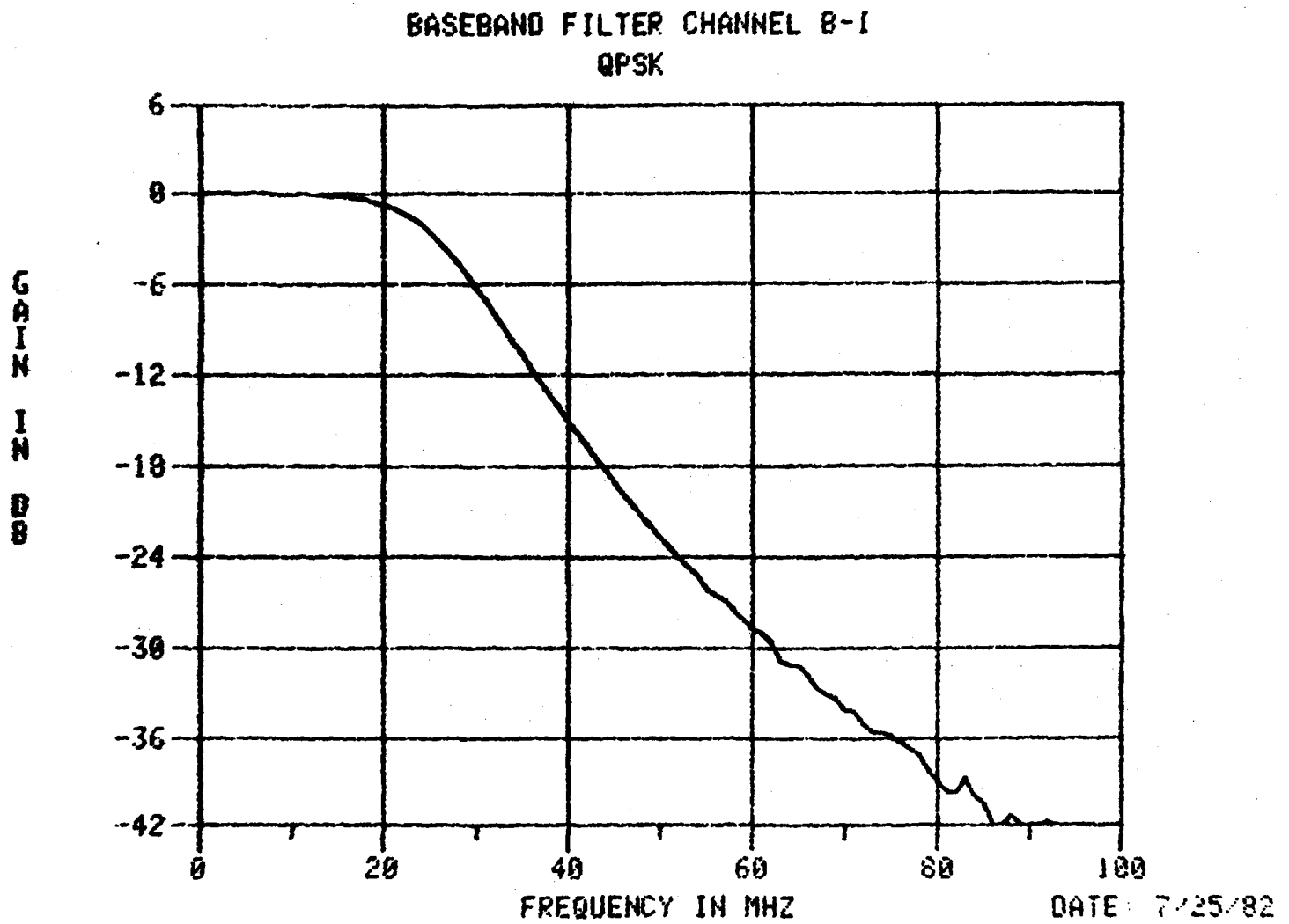

Figure 5-20. Calibration Plot

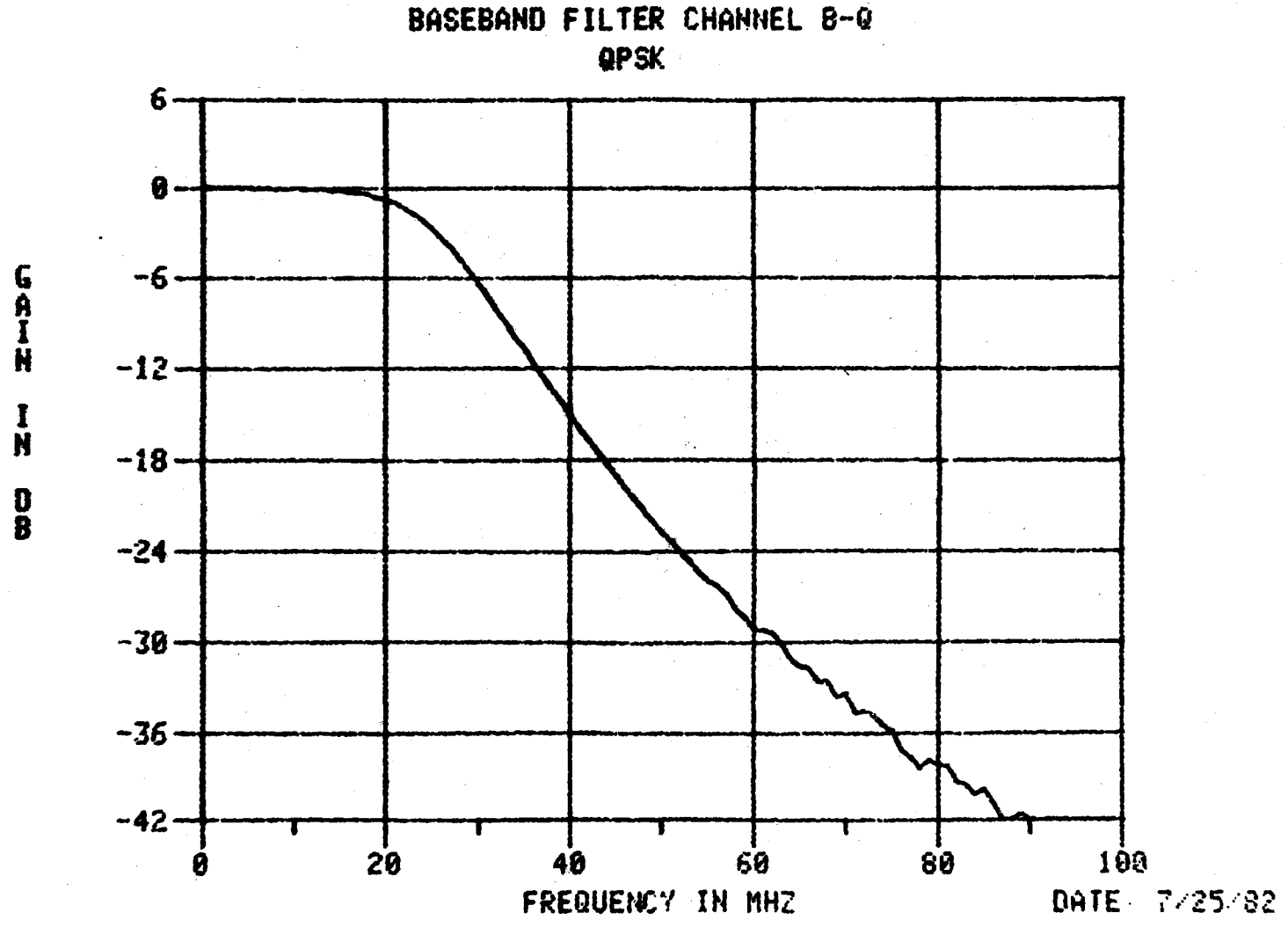

Figure 5-21. Calibration Plot.

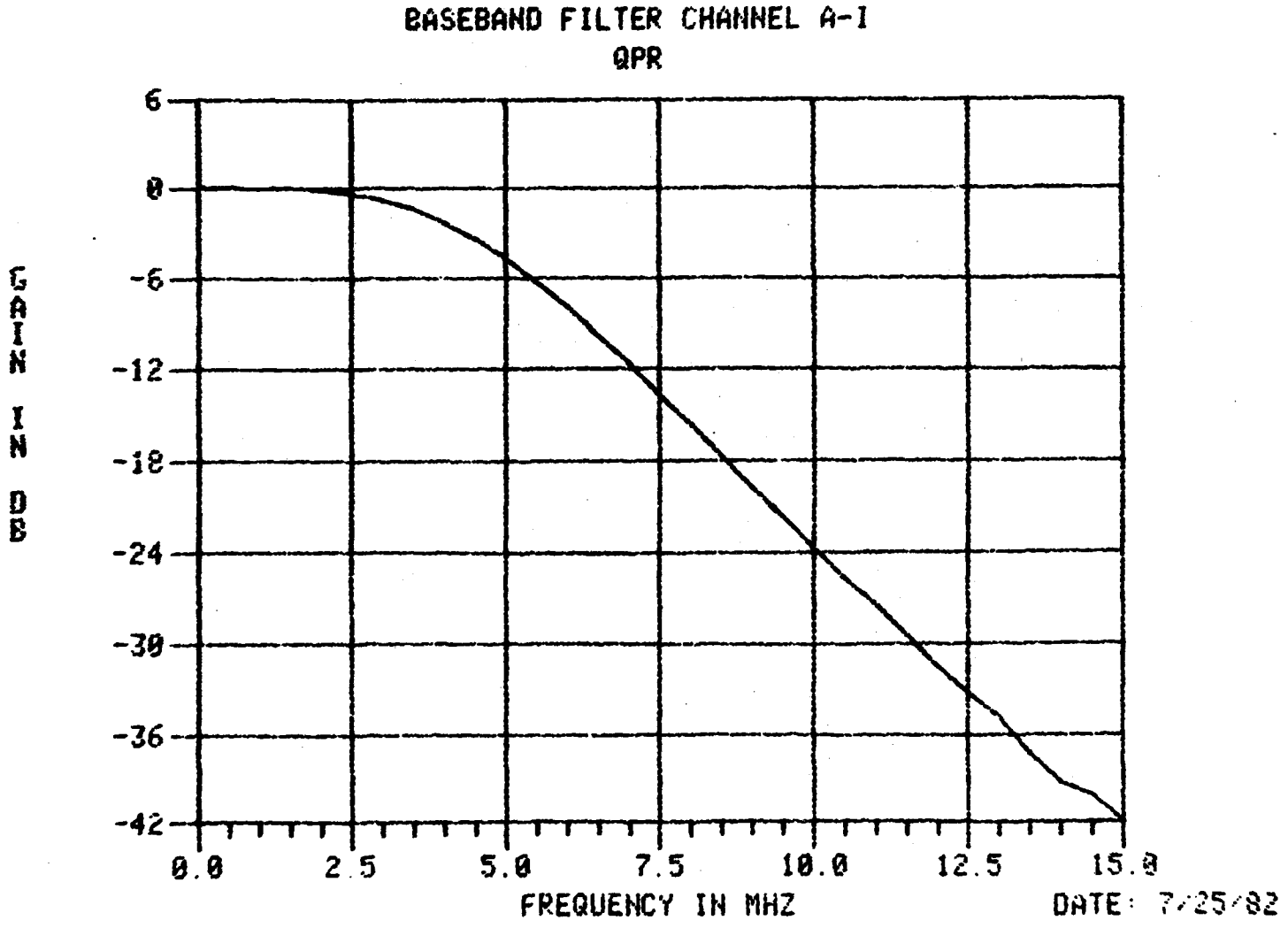

Figure 5-22. Calibration Plot

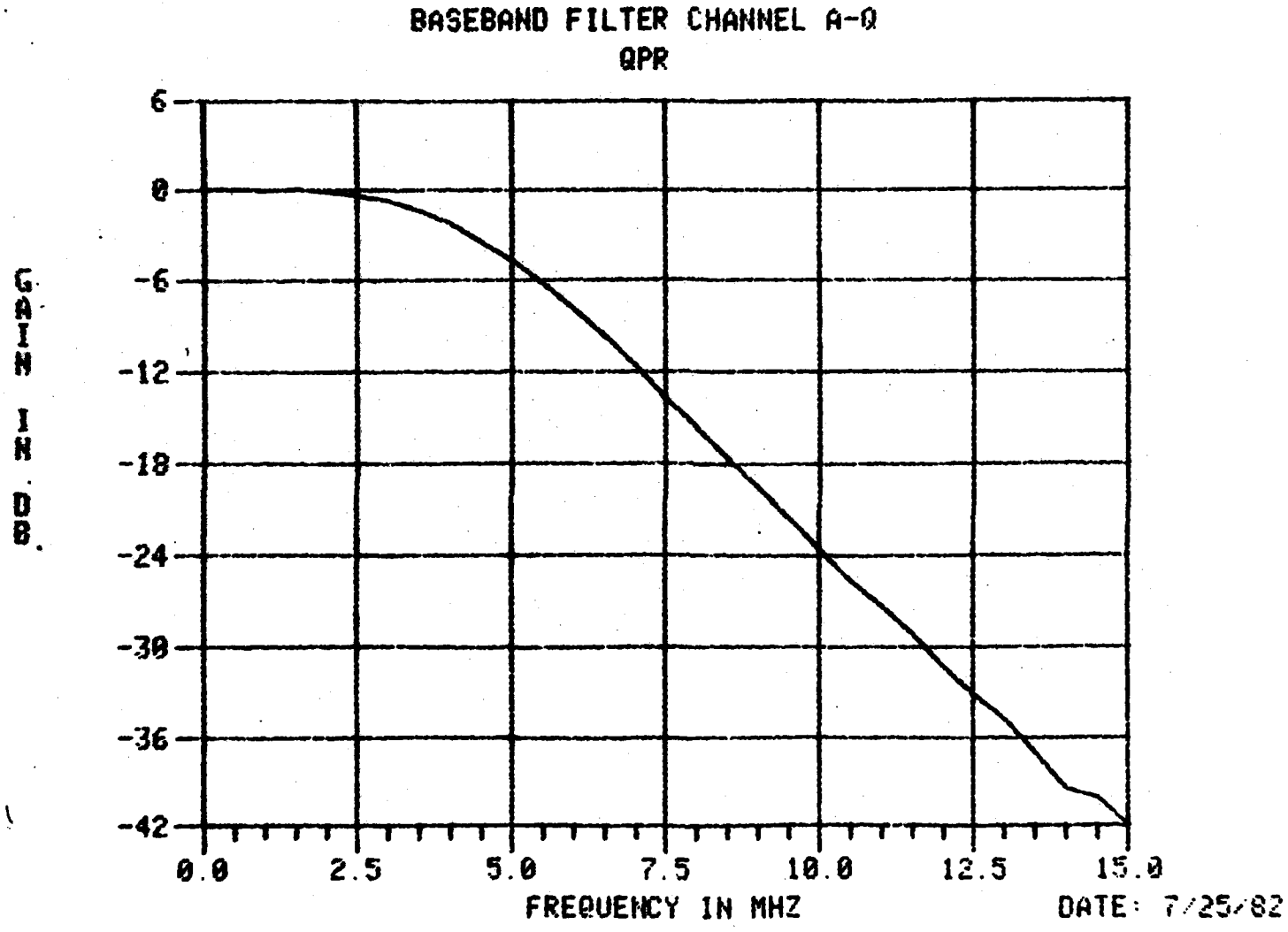

Figure 5-23. Calibration Plot

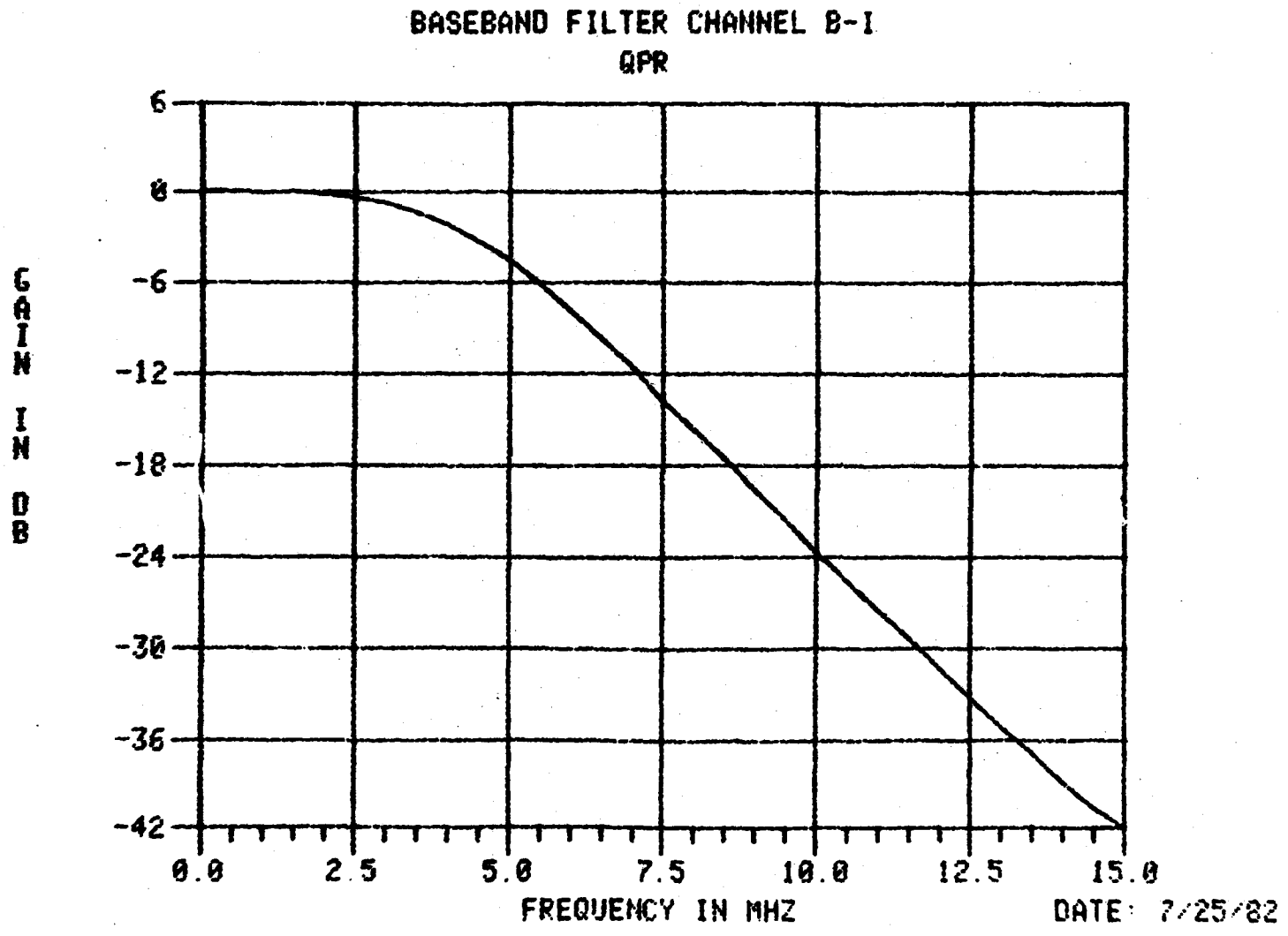

Figure 5-24. Calibration Plot

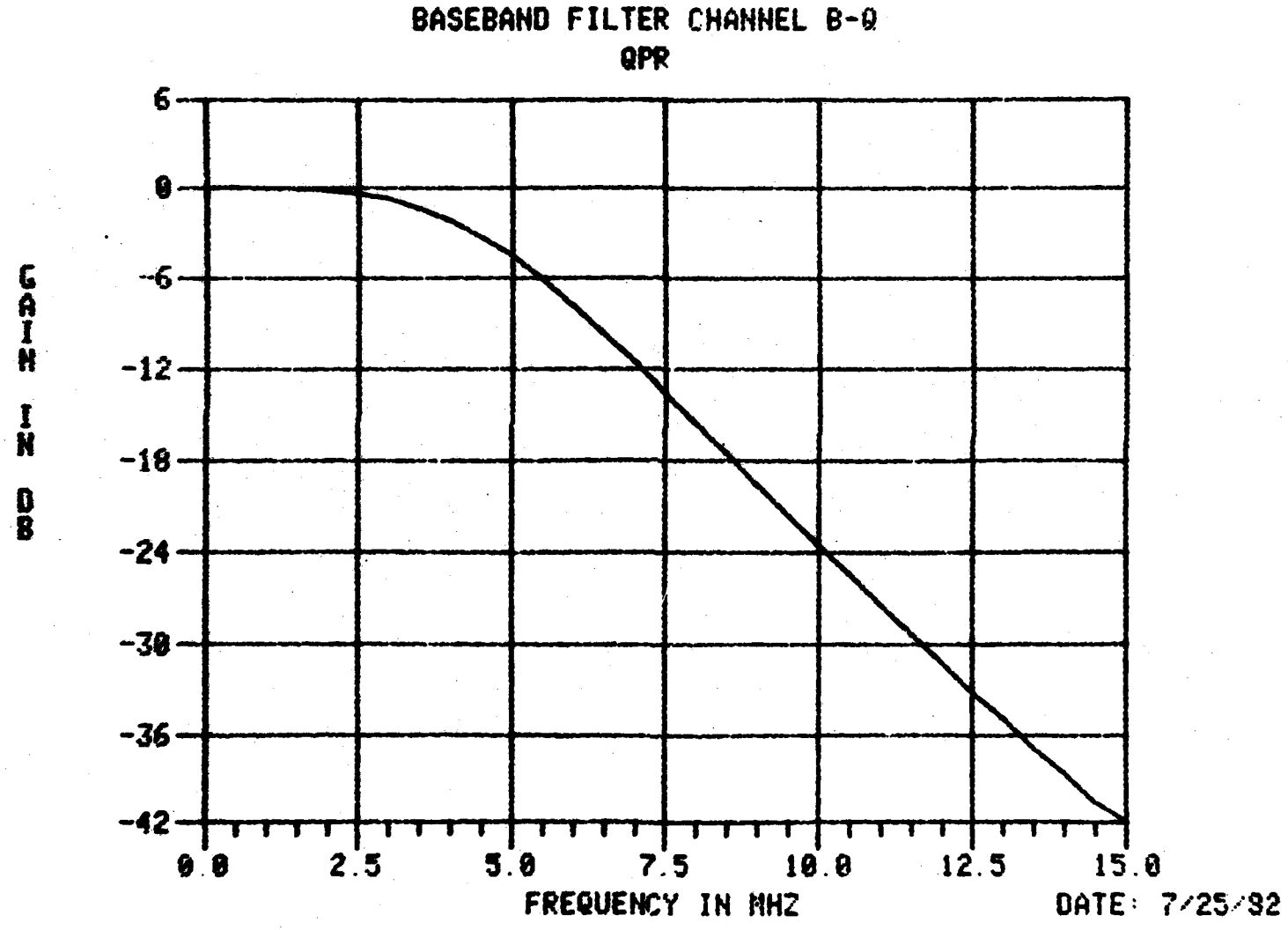

Figure 5-25. Calibration Plot

6.0 SUMMARY

This final report has documented work accomplished under Contract DCA100-81-C-0016. Several major changes and additions were made to the AN/FRC-170(V) hybrid computer simulation to provide a simulation of the radio and channel that realistically models actual electronic circuits of the radio and expected channel characteristics.

During this contract period the simulation was used extensively via the remote terminal at DCEC by Mr. Stanley Soonachan and Dr. Dave Smith to make various simulation studies. Hysterisis runs were made to minimize diversity errors as a function of pseudo error register length and OTM threshold at various secondary tap gains. Studies were made at various Eb/No settings to determine BER vs PER linearity as a function of OTM threshold.

Model enhancements included modeling and simulation of a dual diversity combiner, an improved signal quality monitor, an improved baseband equalizer, and an IF slope equalizer. In addition a TDM framing pattern insertion to the aggregate bit stream was modeled, a hard copy plot of BER vs PER was provided, and a fade outage monitor was simulated. Interactive displays and controls, documented in this report, were developed for the remote user in order to provide complete control and monitoring of the simulation from a remote site. Other capabilities included adaptive threshold

circuits for carrier recovery, clock recovery, and data slicing and channel model enhancements.

APPENDIX A

THE SIMULATION OF DYNAMIC SYSTEMS WITH THE INTEL 2920 SIGNAL PROCESSOR

The Intel 2920 is "touted" as a single chip signal processor designed specifically to function in real time applications. However, it offers exceptional opportunities in simulation applications because it's "ideally" suited to simulate transfer-function models of dynamic systems - as well as being suited for performing a variety of non-linear function operations. The simulation is accomplished digitally. All the required analog interface is onboard the single chip. Thus, single chips can be used to simulate whole classes of dynamic sub-systems, which is extremely attractive for "off-loading" general purpose processors or partitioning larger problems for easier management.

The AN/FRC-170(V) simulation application for the 2920 was the modified 5th order elliptic receiver filter specified by

$$H(s) = \frac{1464}{s + 1464} * \frac{0.17596(s^2 + 78005.10^2)}{s^2 + 1908.9s + 27451*10^2} * \frac{0.1847(s^2 + 18341*10^3)}{s^2 + 539.39s + 33876*10^2} \quad [1]$$

where H(s) represents the simulation model. The real-time model of the original system is 26,112 times faster. The filter frequency response is given in Figure A-1.

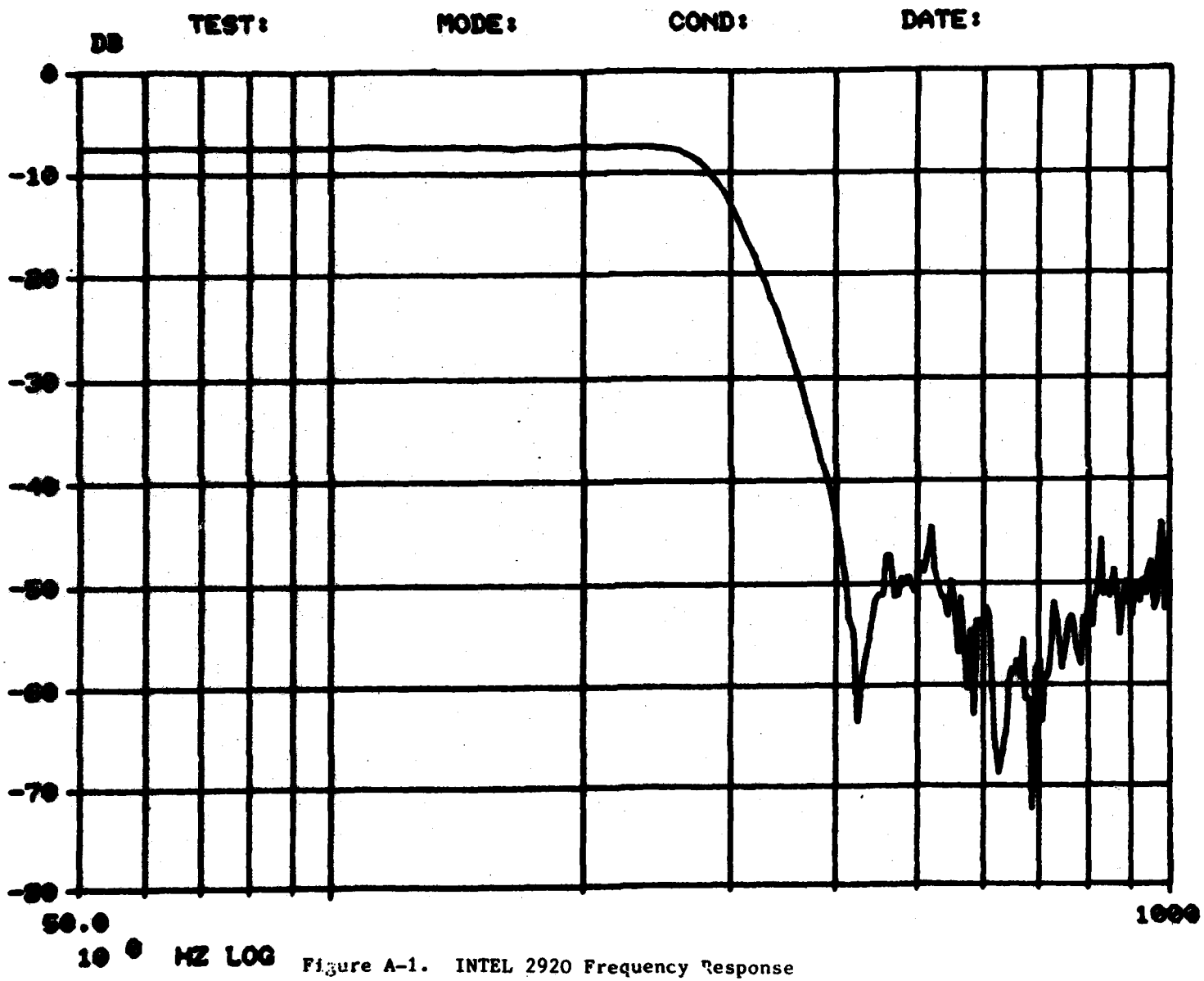

Figure A-1. INTEL 2920 Frequency Response

One possible procedure for implementing 2920 simulations of dynamic systems follows. The receiver filter model is used as the example.

- Step 1. From the real-time system requirements, formulate a simulation model scaled to function at simulation speeds. For the receiver filter, the H(s) of [1] was the resulting simulation model.

- Step 2. With a knowledge of simulation signal frequencies, select a digital "2920" sample frequency, f_s. The ratio of f_s to signal frequencies should be in the order of 10 or 20 to 1 for most applications. In non-critical applications, that ratio could be reduced.

- Step 3. With $T_s \triangleq 1/f_s$, the H(z) digital model must be derived from the H(s) model. The usual techniques are impulse or step-invariant, bilinear transform or pre-warped frequency response, etc. Applying a pre-warped bilinear transform match at $f_{\pm}$ 352 Hz with an f_s = 9750 Hz, the digital model derived from the H(s) of [1] is

$$H(z) = \frac{0.70114(1+z^{-1})}{1-0.85978z^{-1}} \cdot \frac{0.16245(1-1.9189z^{-1}+z^{-2})}{1-1.7958z^{-1}+.82215z^{-2}} \cdot \frac{0.18682(1-1.8144z^{-1}+z^{-2})}{1-1.9117z^{-1}+.94641z^{-1}} \quad [2]$$

- Step 4. Formulate a simulation diagram of cascaded minimum order sections. In this case, a 1st and two 2nd order sections were used.

- Step 5. Using an Intel development system, key in a 2920 assembly language program file for the model of [2]. For H(s) models, only 3 subprograms are required: A "canned" input routine; a "canned" output routine; and the H(z) program consisting of just 3 instruction types: (loads, subtracts, and adds with shifts). With the program loaded, invoke the 2920 assembler to obtain a hex file (machine coded EPROM file). Intel offers several aids for this process; such as editors, code generators, etc.

- Step 6. Simulate the hex program of Step 5 with a software simulator to verify the H(z) model.

- Step 7. After verifying the hex file by simulation, use an Intel development system with a PROM burner to program the 2920 EPROM.

- Step 8. With a 2920 breadboard, test and evaluate the simulation model using hardware instrumentation. The 2920 receiver simulation was implemented with this procedure and proven to represent the simulated receiver by obtaining a frequency response with the HP 5451B digital spectrum analyzer-while the chip was operating.

  With time, experience and continual improvement, the 2920 (or similar type chips) could prove to be extremely useful in simulation applications. It is possible that demand could justify a completely automated development system program that would produce a fully programmed 2920 from a given H(z) or possibly even an H(s) model.

APPENDIX B

ANALOG COMPUTER DIAGRAMS FOR AN/FRC-170(V) HYBRID COMPUTER SIMULATION

LARMA RADIO SIMULATION

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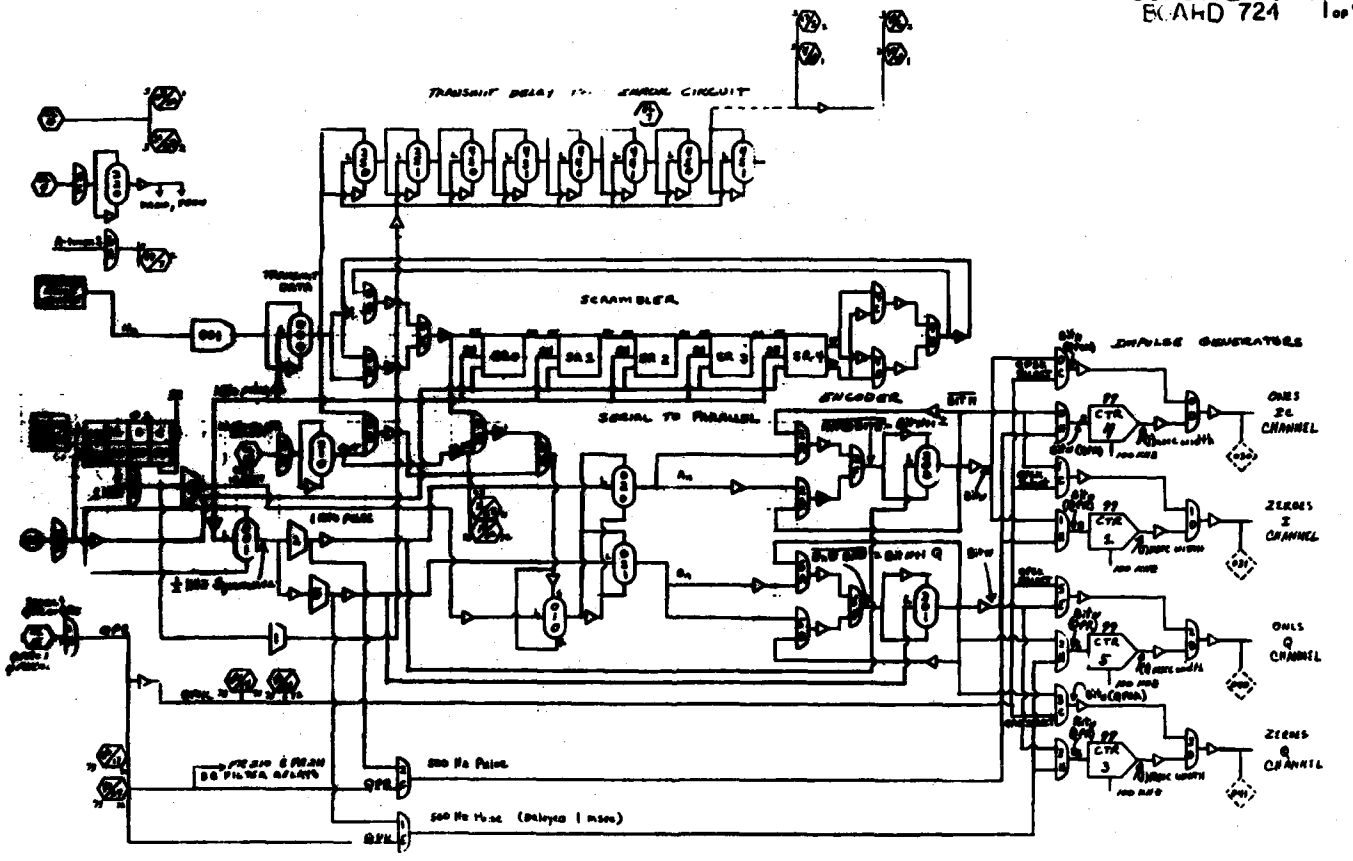
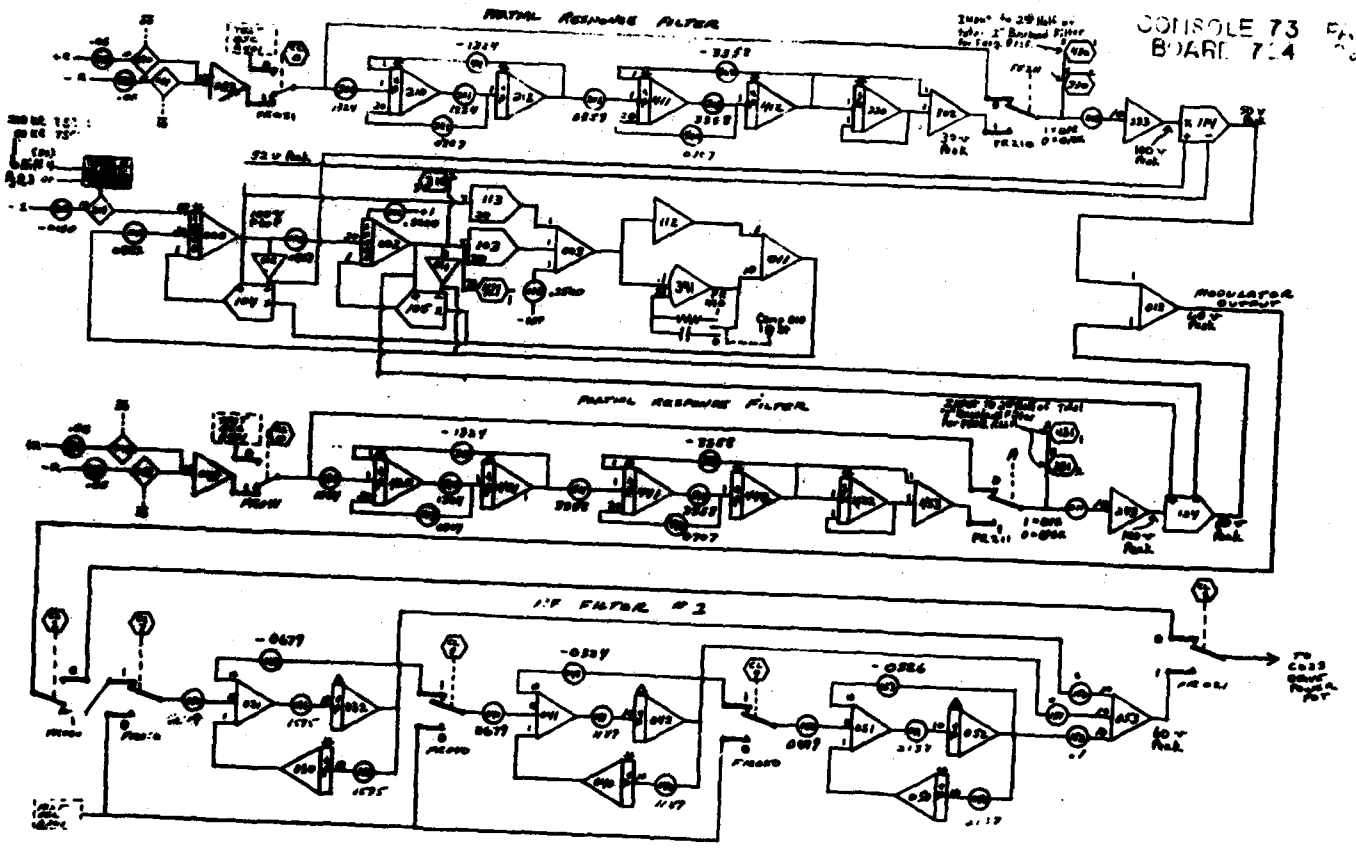
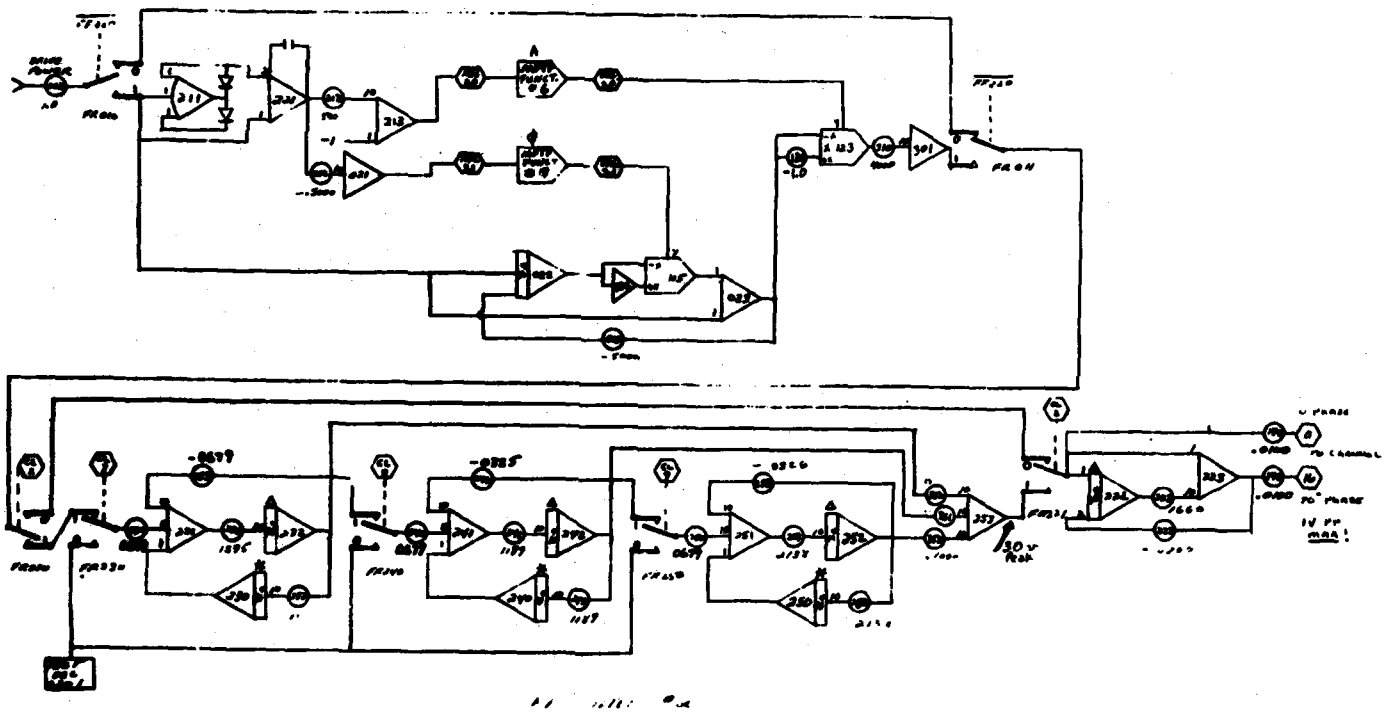




NOTE : * INDICATES PIN IS INPUT TO IC
△ INDICATES PIN IS INPUT TO IC 5 FOR HDI WIRE TEST



NOTE: * - PRIM INPUT TO IC
Δ - PIOS INPUT TO IC

CHANNEL MEDIA MODEL

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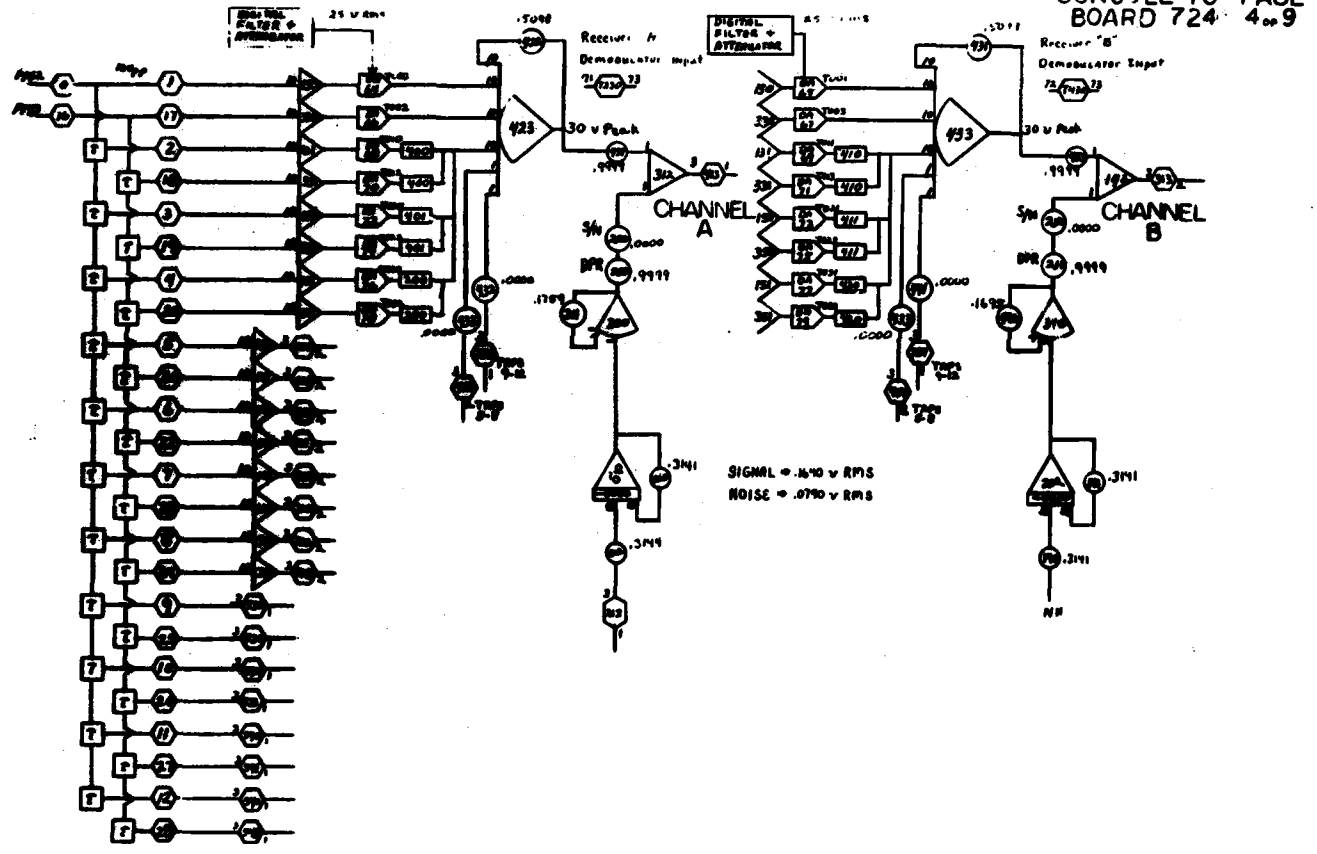
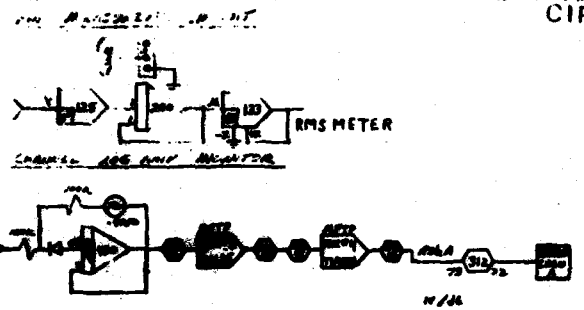
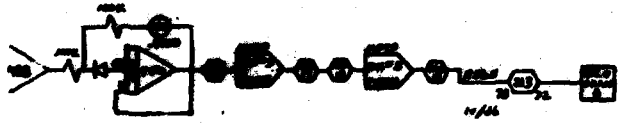
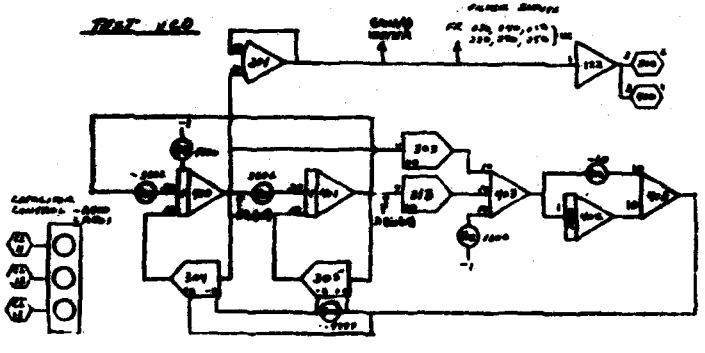
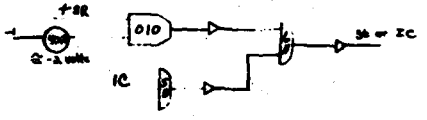


TEST AND DISPLAY
CIRCUITS

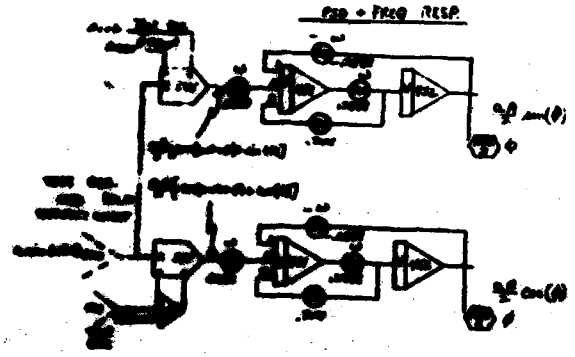


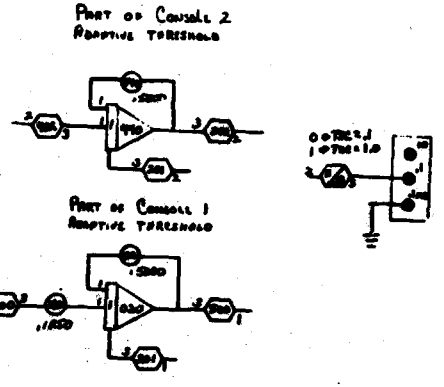






B-6

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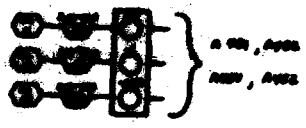
ADAPTIVE THRESHOLD
PART OF CONSOLE 1
ADAPTIVE THRESHOLD



MEASUREMENT AND TEST SELECTION

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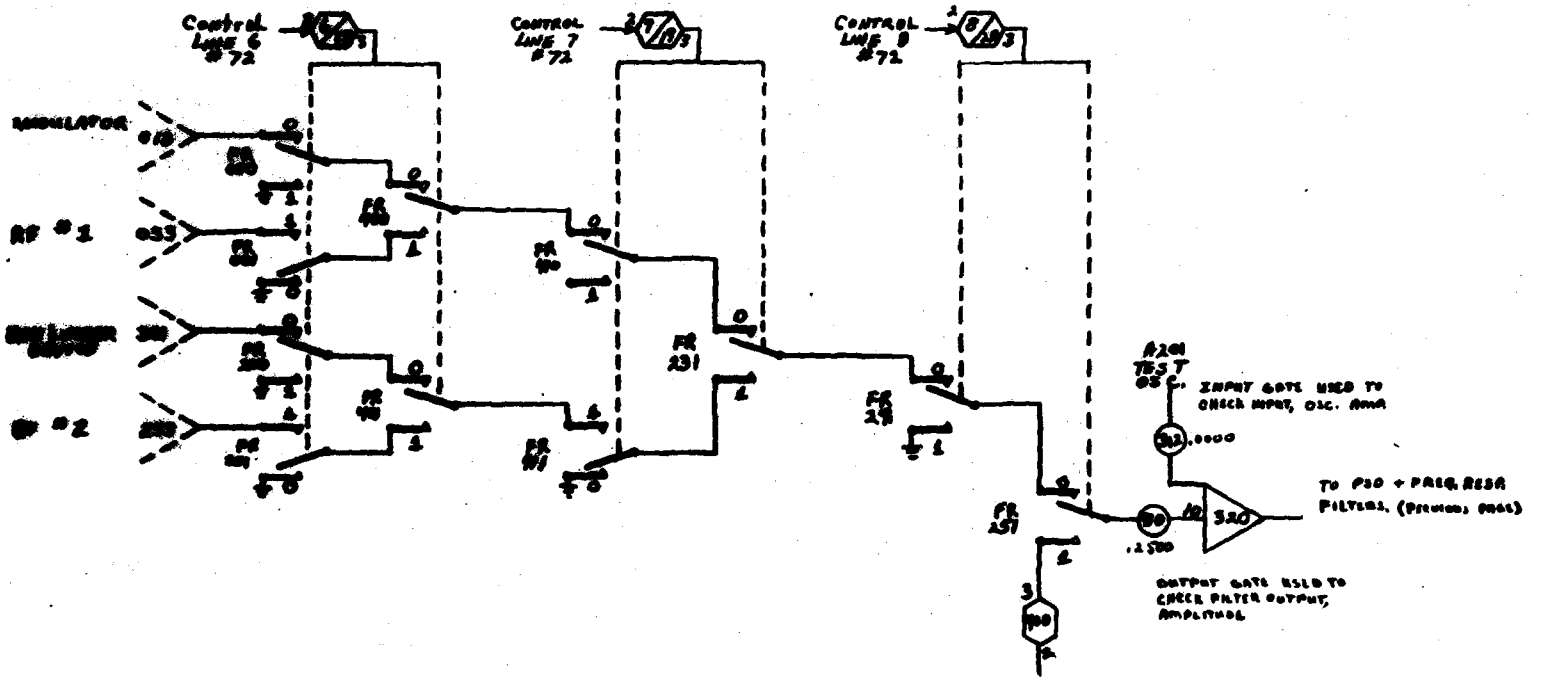
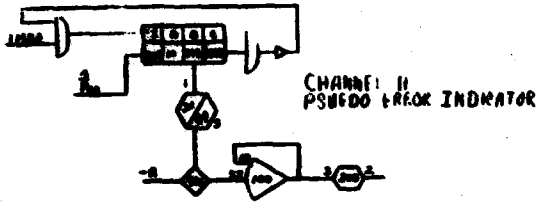
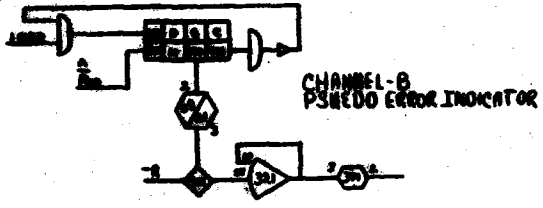
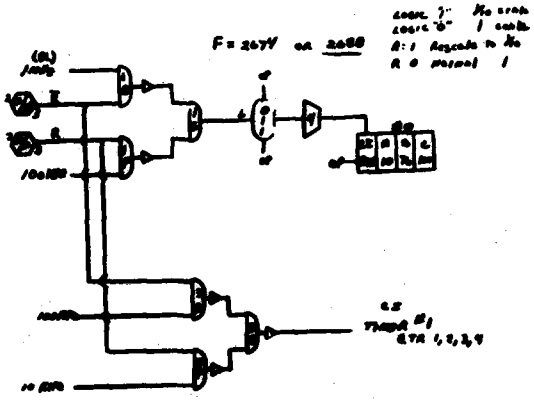




CHANNEL II
PSUEDO ERROR INDICATOR

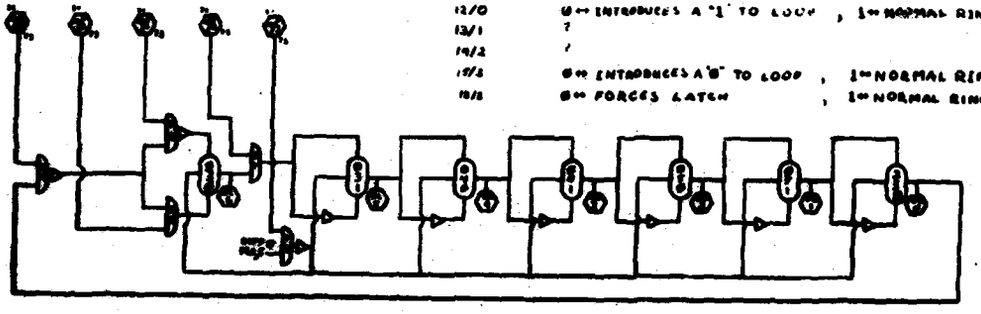


CHANNEL-B
PSUEDO ERROR INDICATOR



CONSOLE 73 RING COUNTER

TRUNK	FUNCTION
12/0	0= INTRODUCES A "1" TO LOOP , 1= NORMAL RING COUNTING OPERATION
13/1	?
14/2	?
15/3	0= INTRODUCES A "0" TO LOOP , 1= NORMAL RING COUNTING OPERATION
16/4	0= FORCES LATCH , 1= NORMAL RING COUNTING OPERATION



IF FILTER 3

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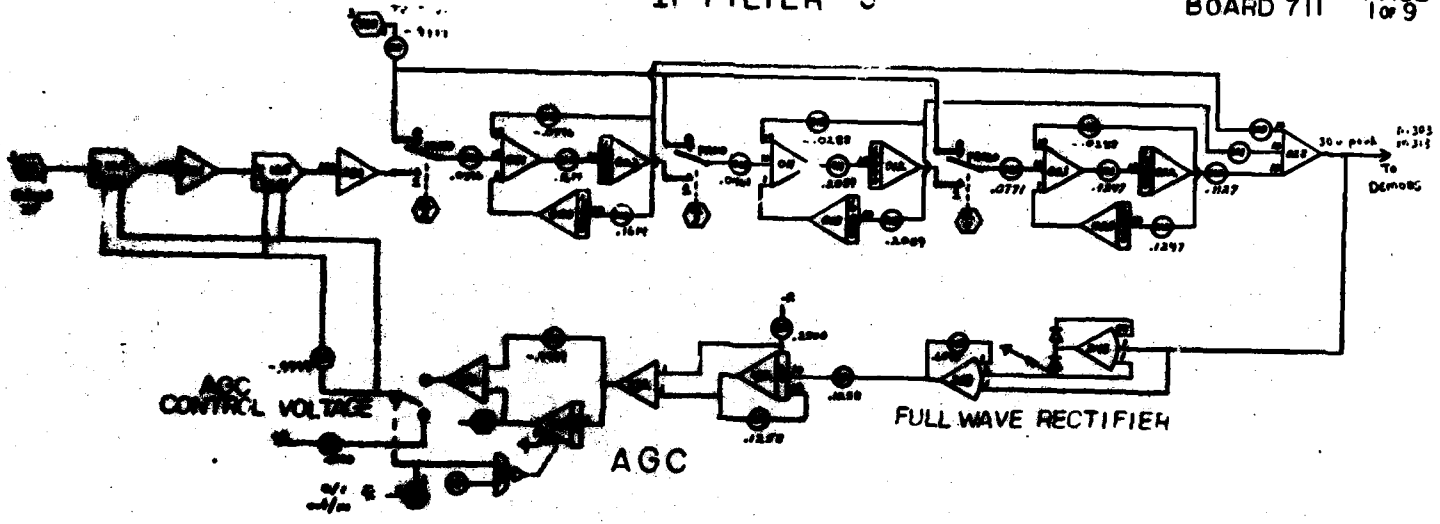
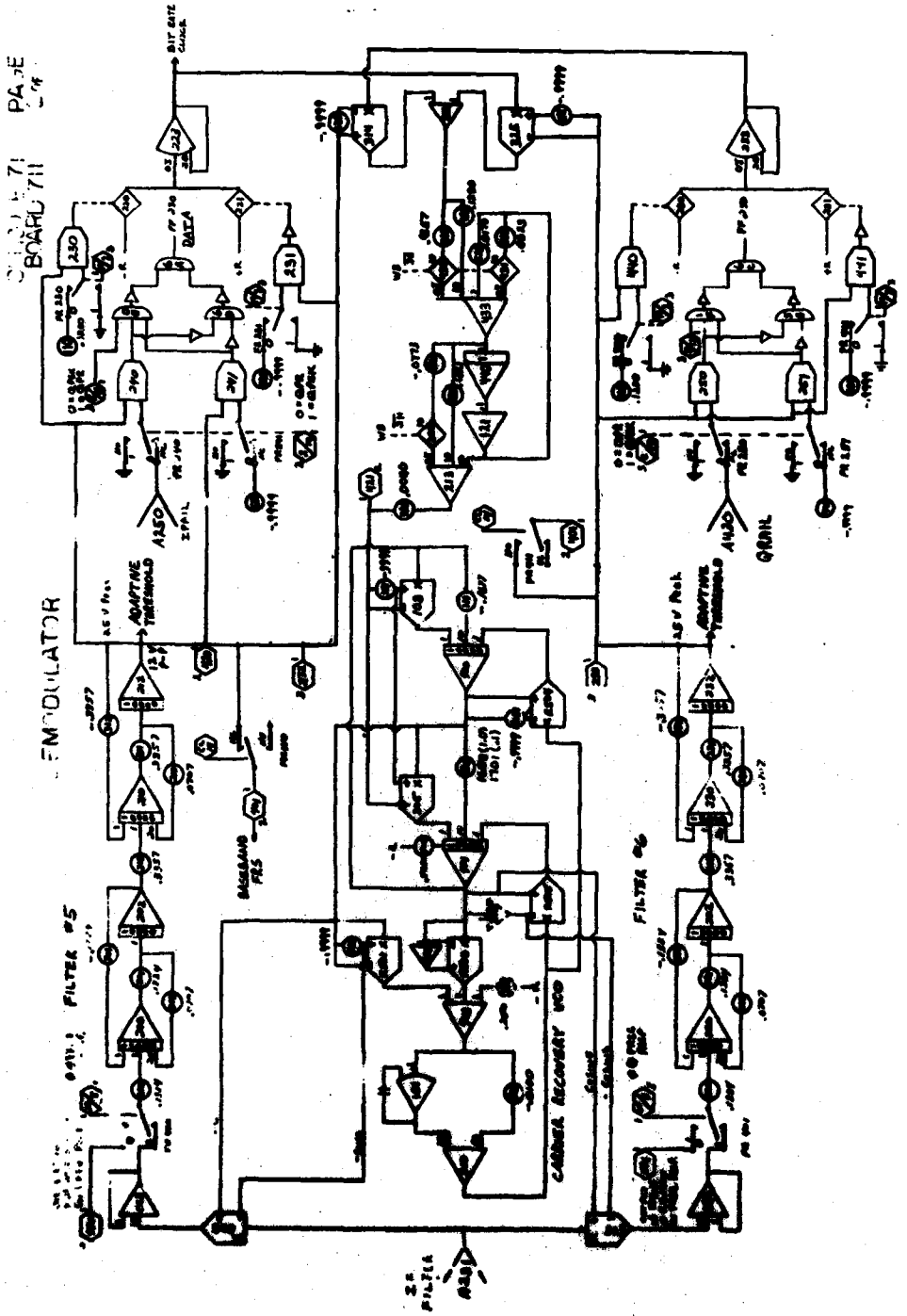
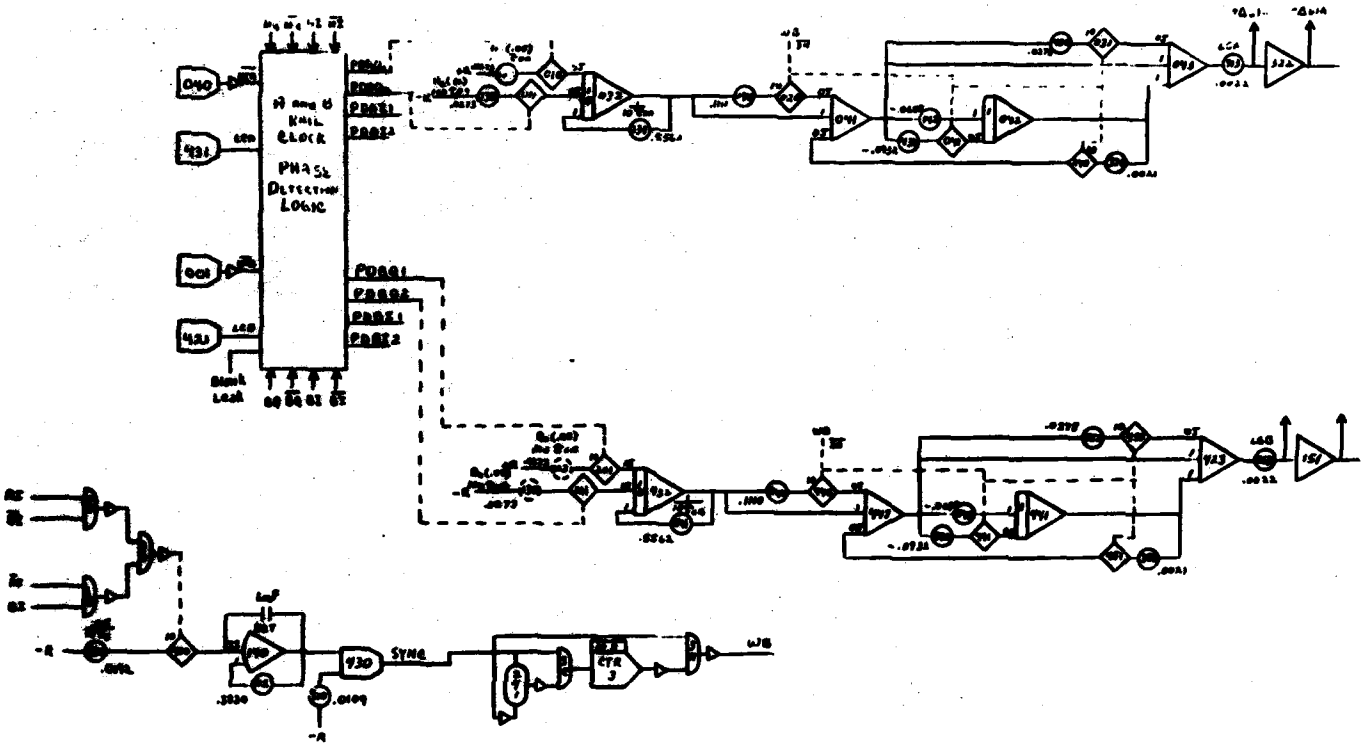
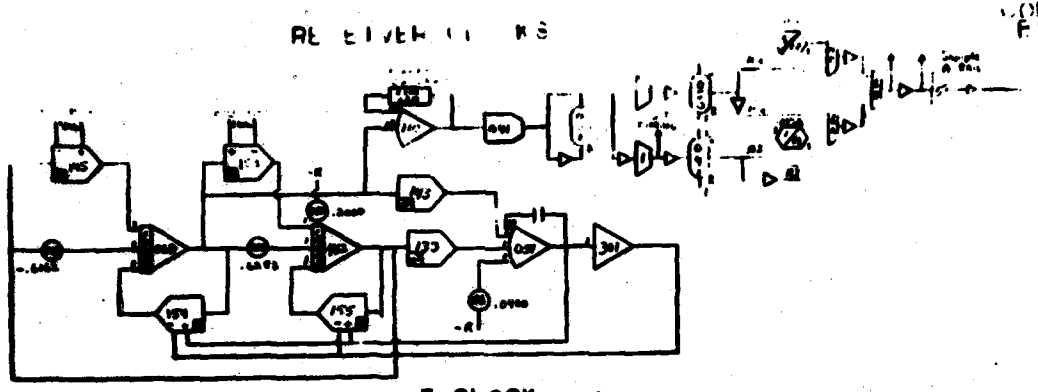




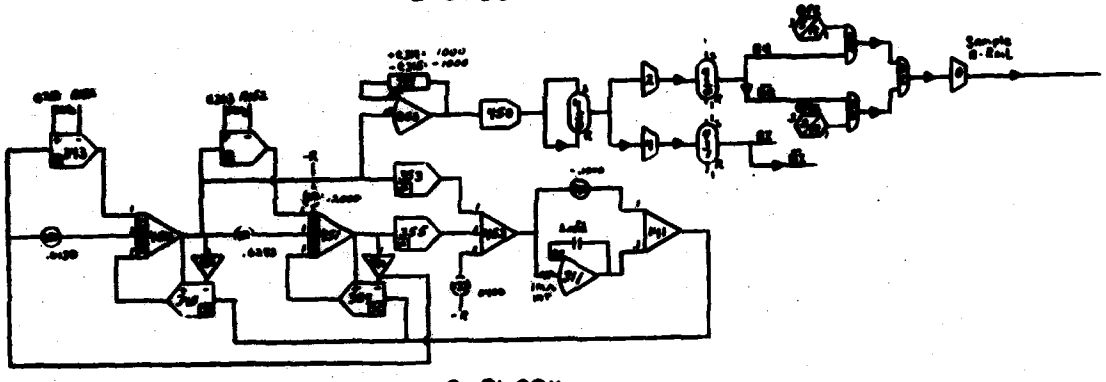
CLK / CLK RECOVERY PLL



LOCK DETECTION



I-CLOCK

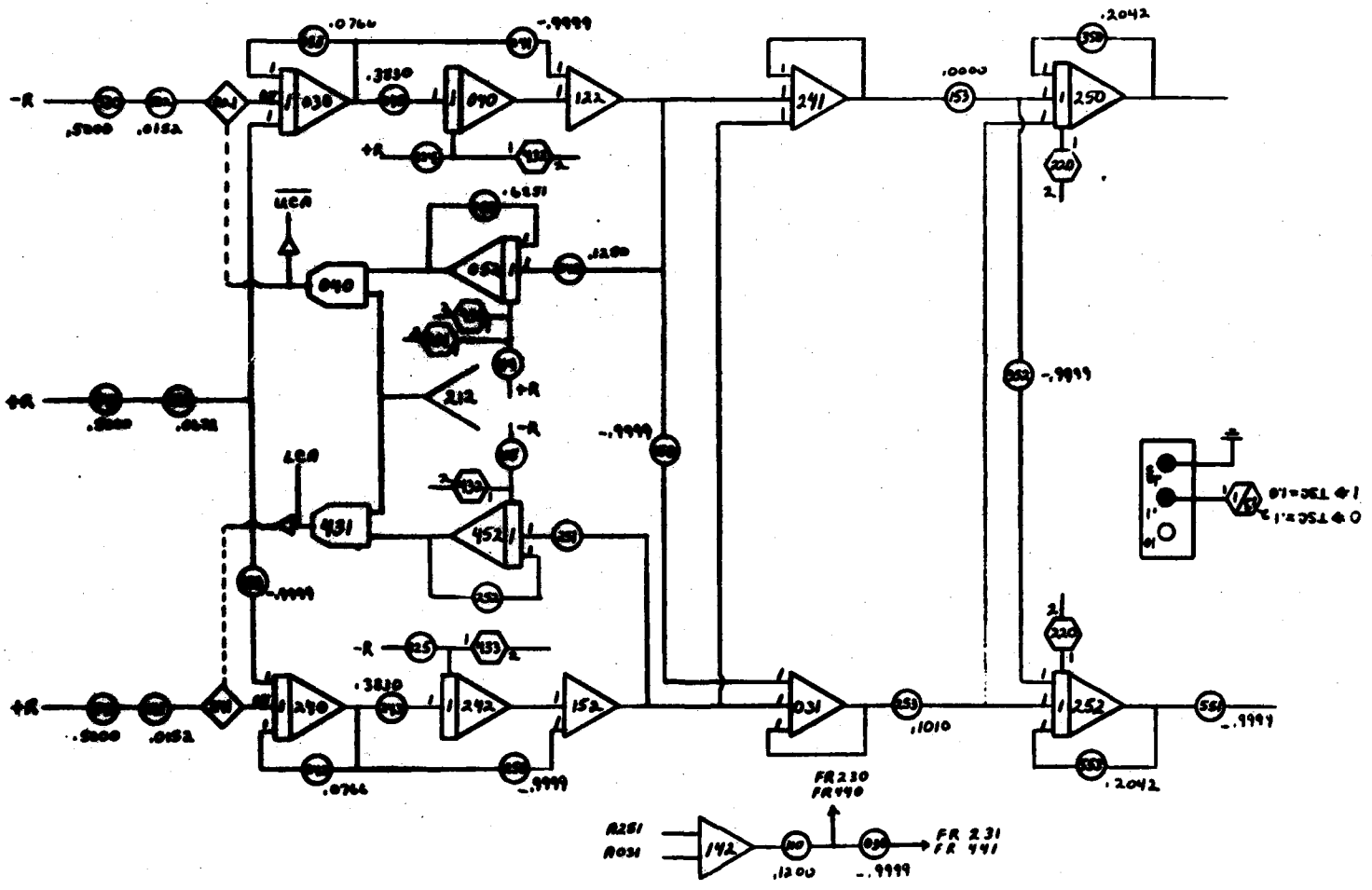


Q-CLOCK

ADAPTIVE THRESHOLD

CONSOLE 71 PAGE
BOARD 711 5.9

I-RAIL



ADAPTIVE THRESHOLD

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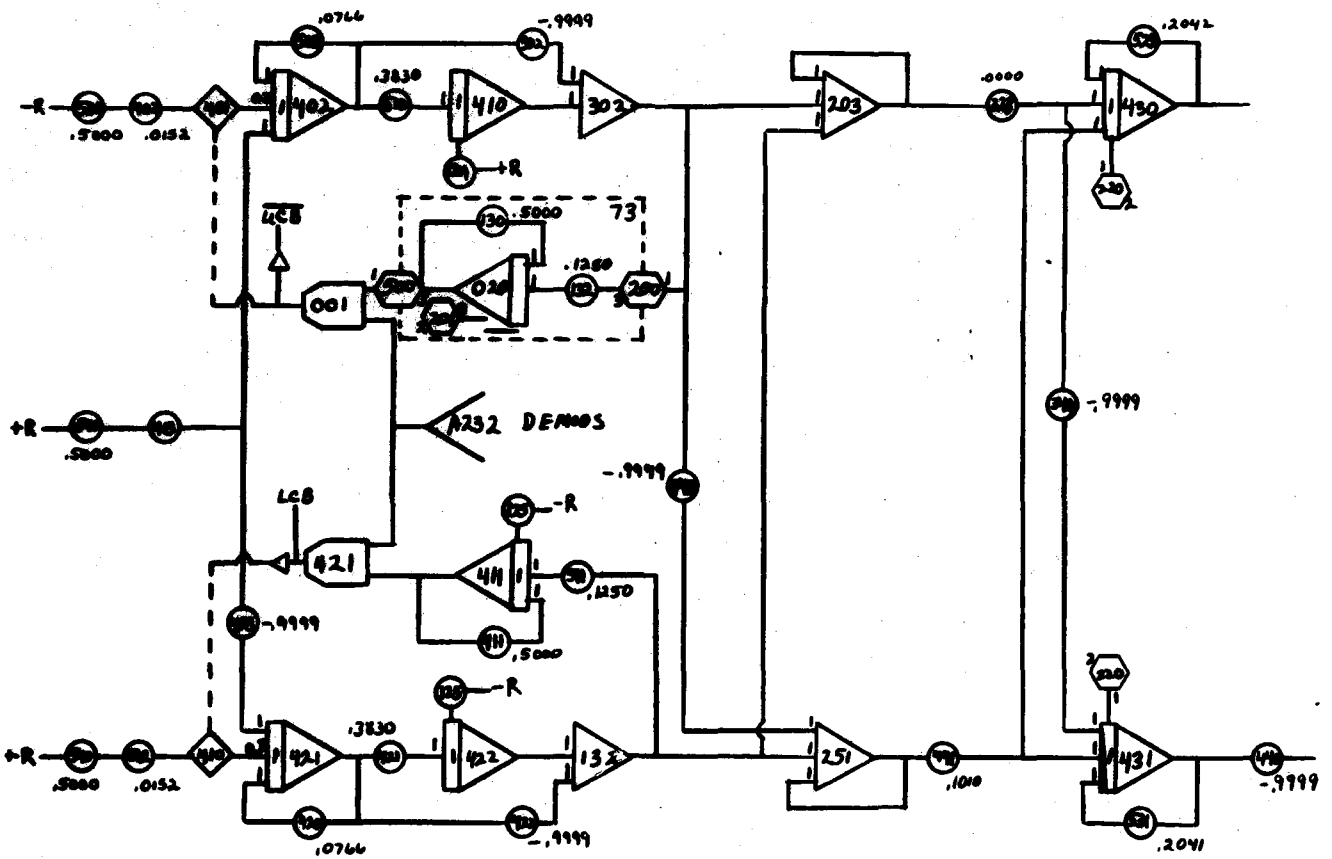
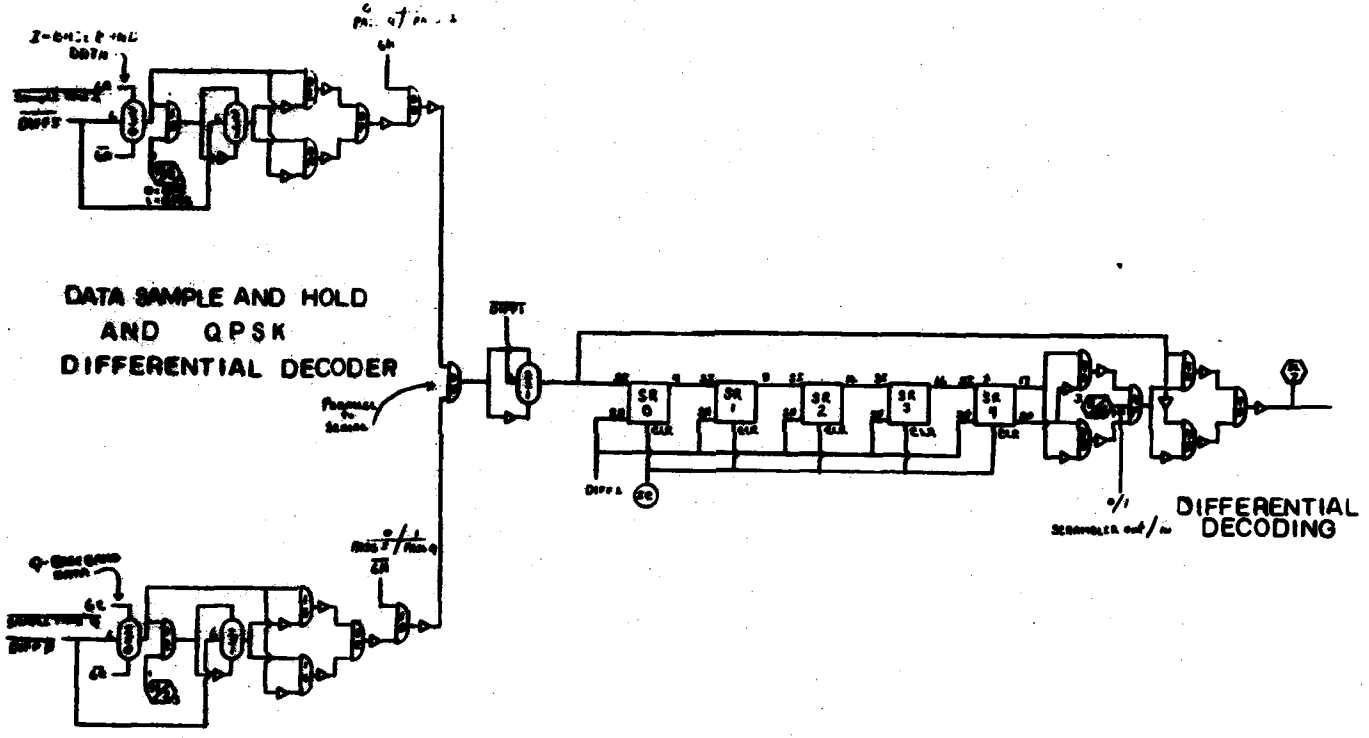
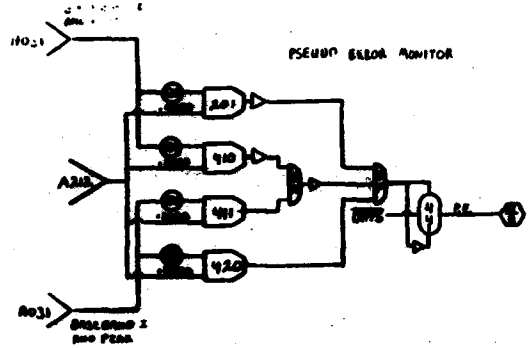
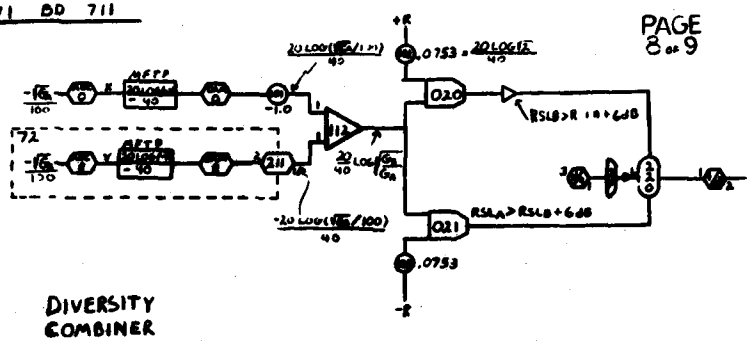
Q-RAIL

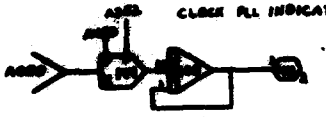


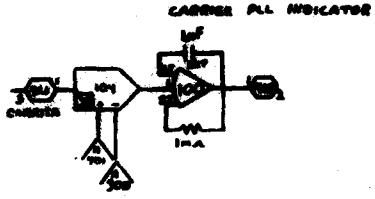
DATA REGENERATION

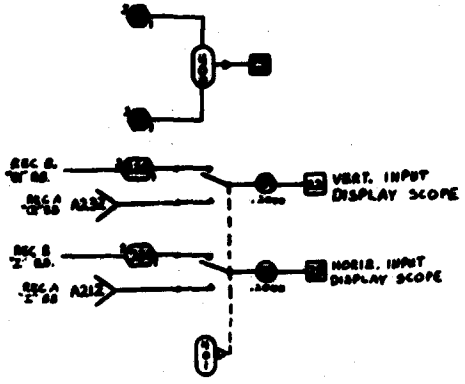












TEST AND MONITOR CIRCUTS

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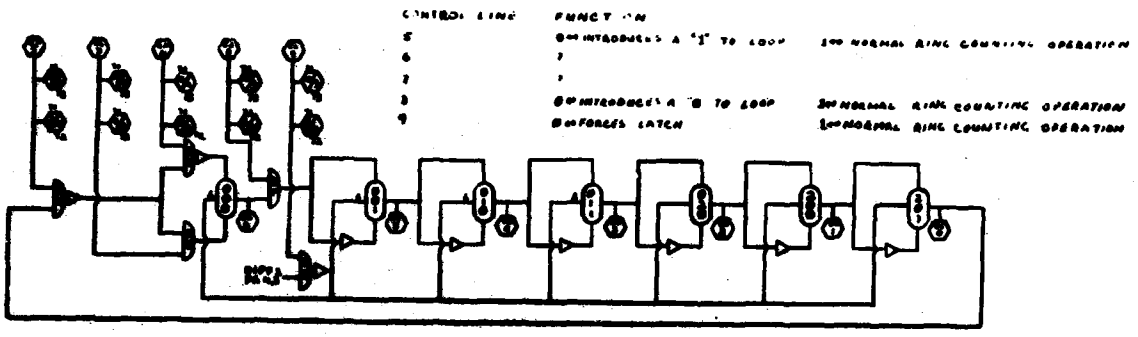
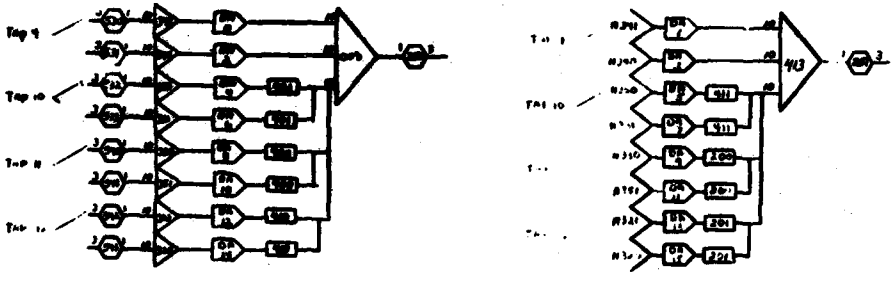


CHANNEL MEDIA MODEL



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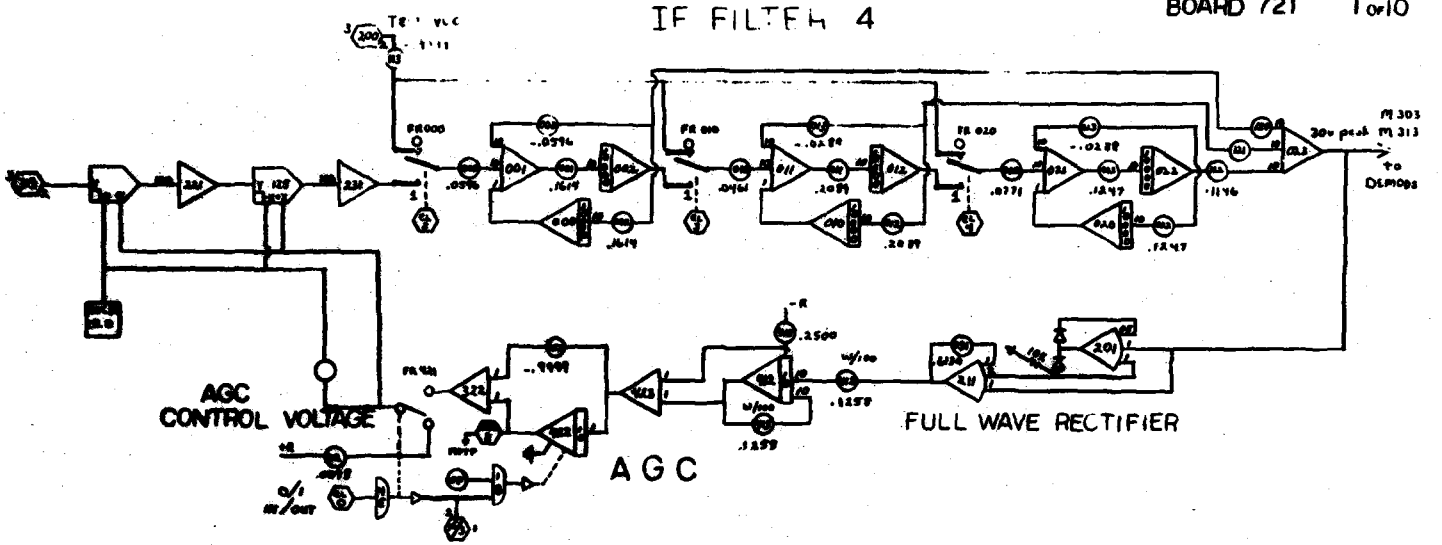
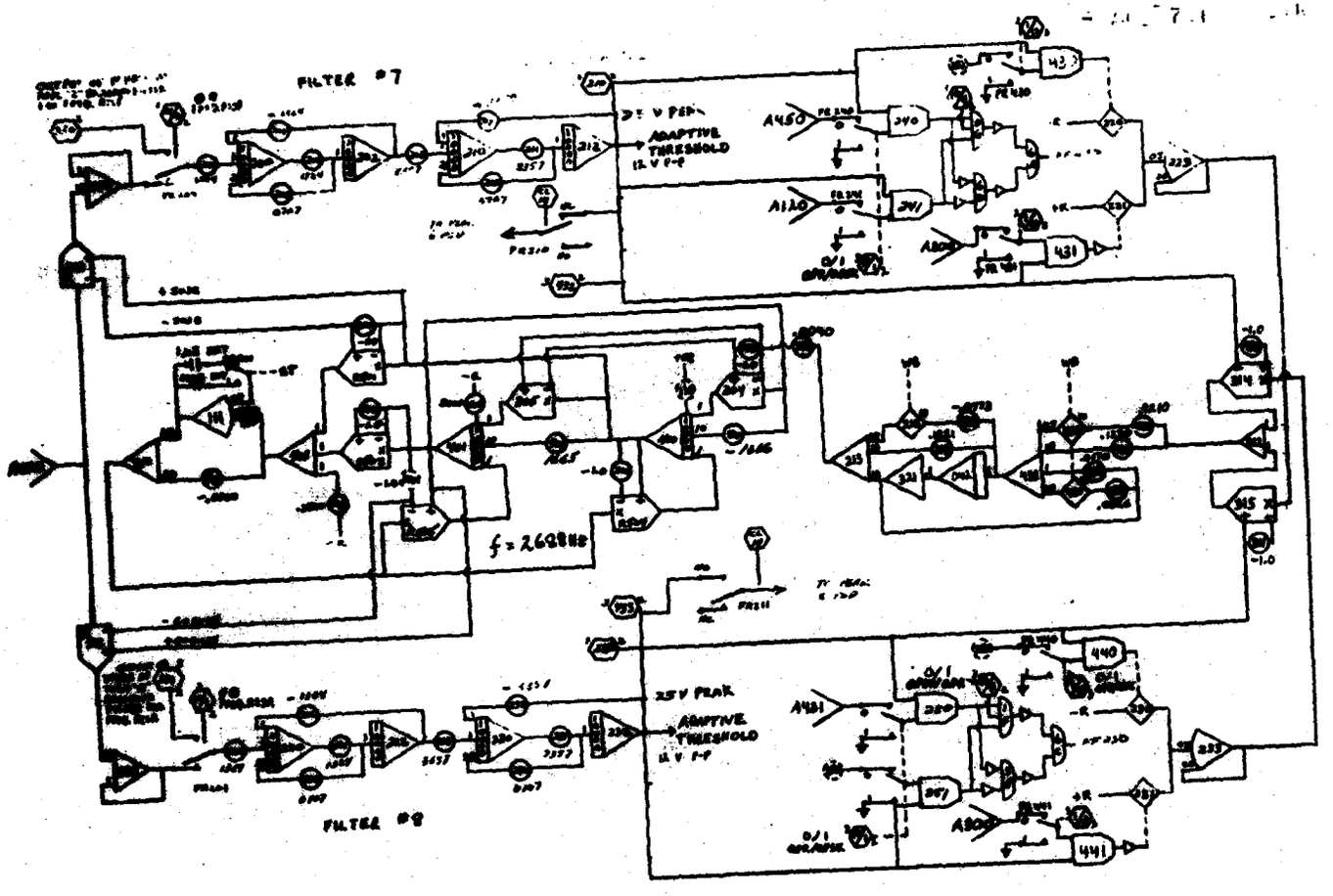
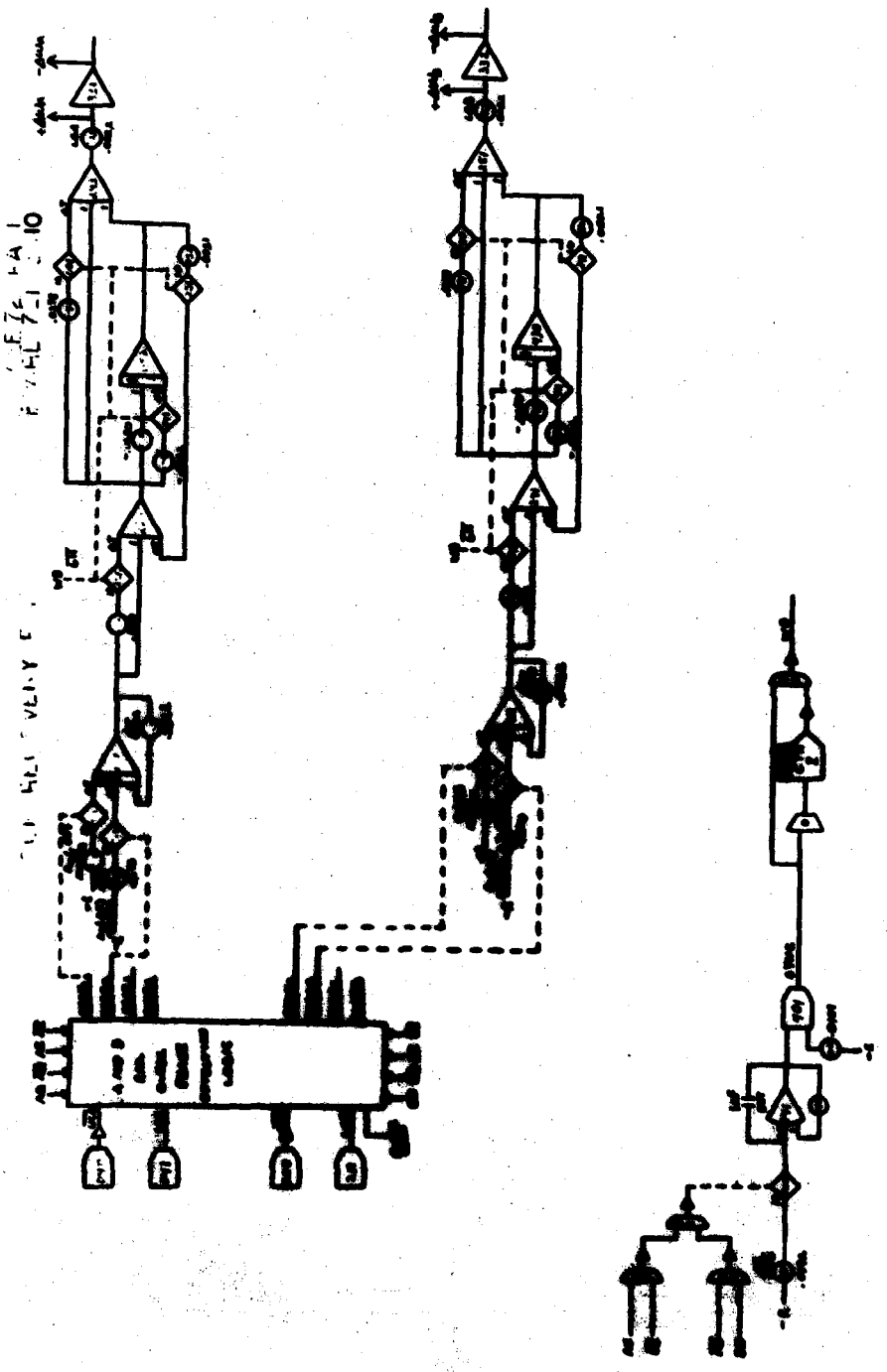
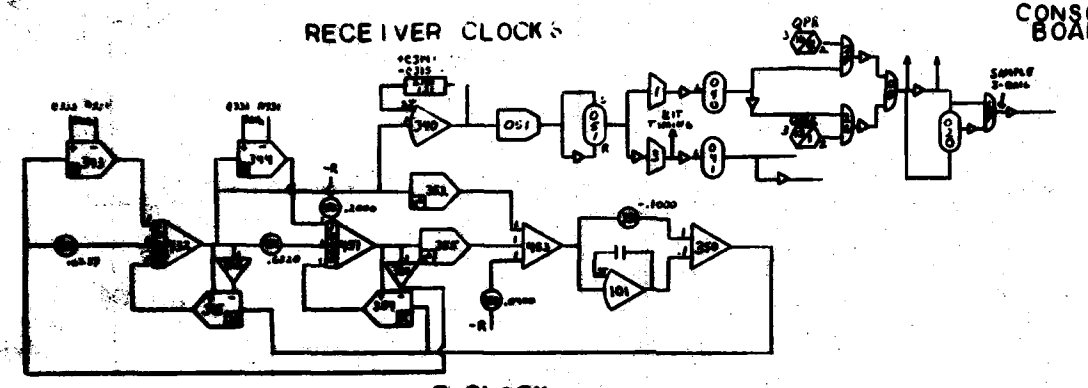


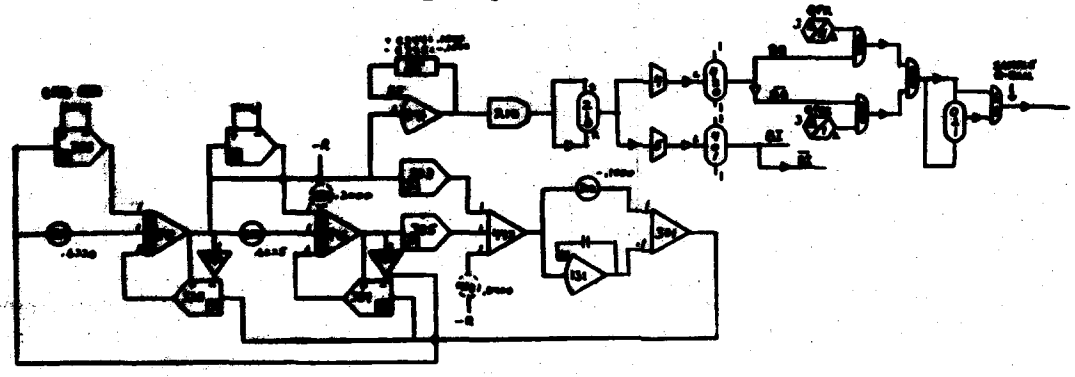

FILTER #7
ADAPTIVE THRESHOLD
FILTER #8
ADAPTIVE THRESHOLD



RECEIVER CLOCKS



I-CLOCK



Q-CLOCK

ADAPTIVE THRESHOLD

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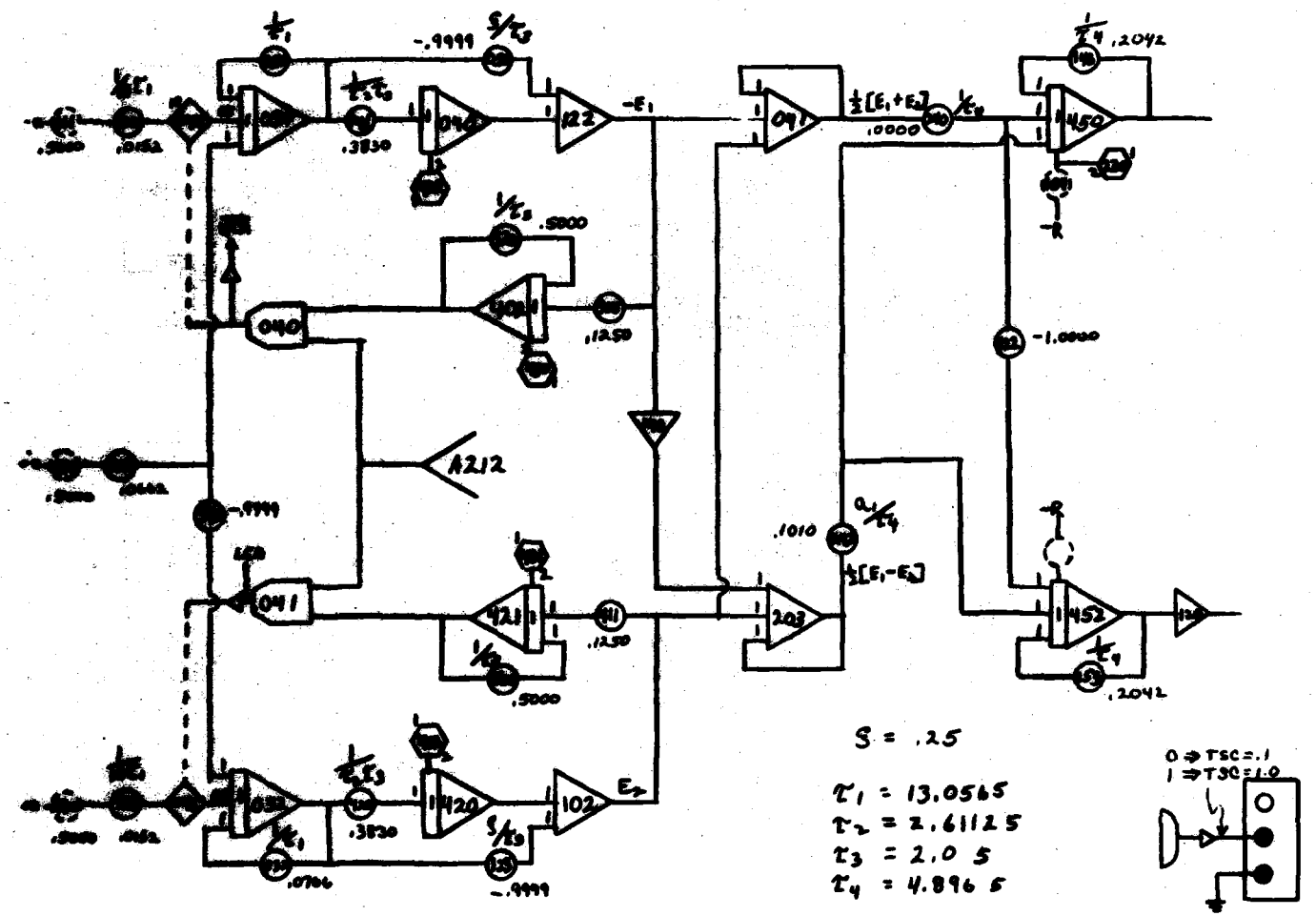
I-RAIL



ADAPTIVE THRESHOLD

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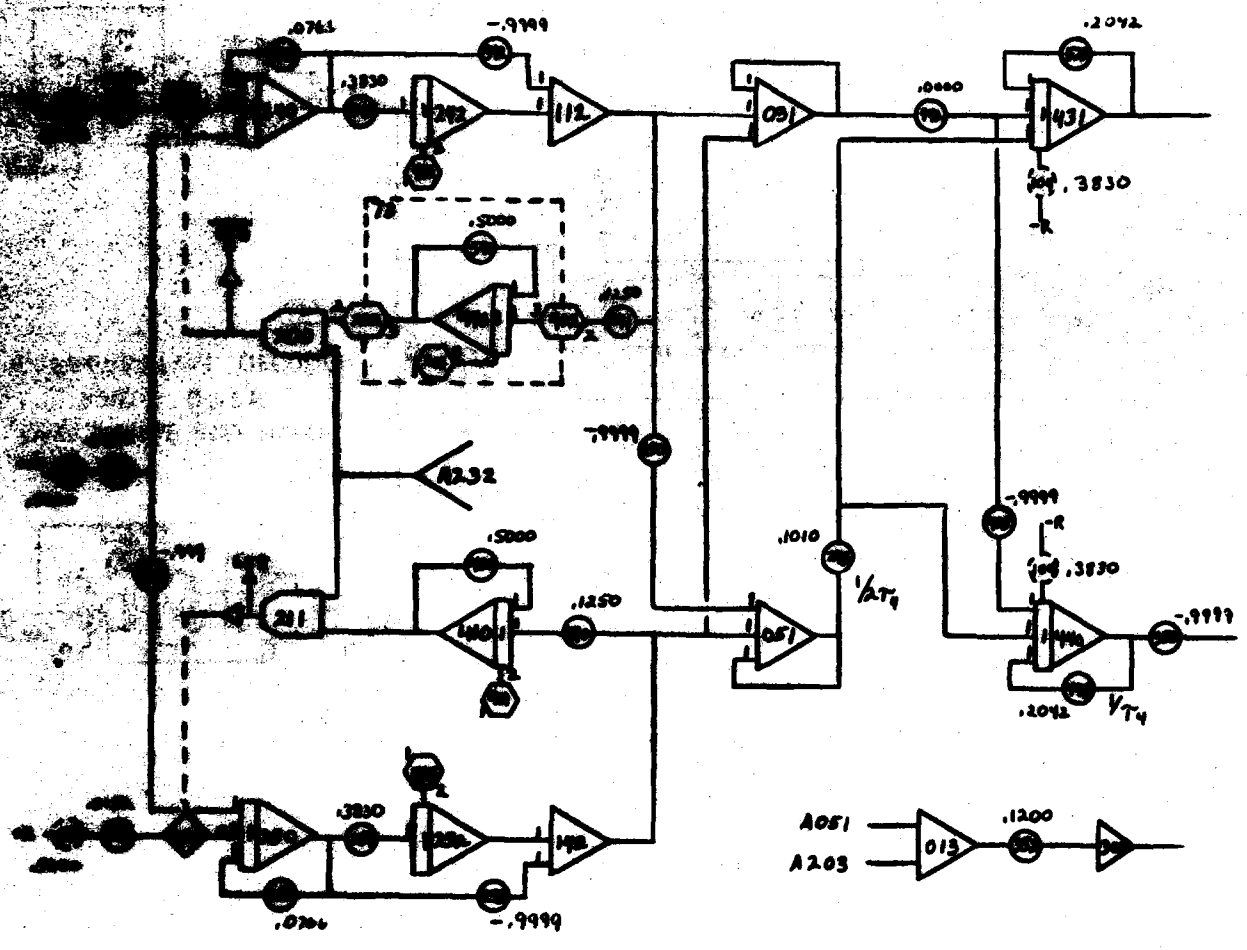
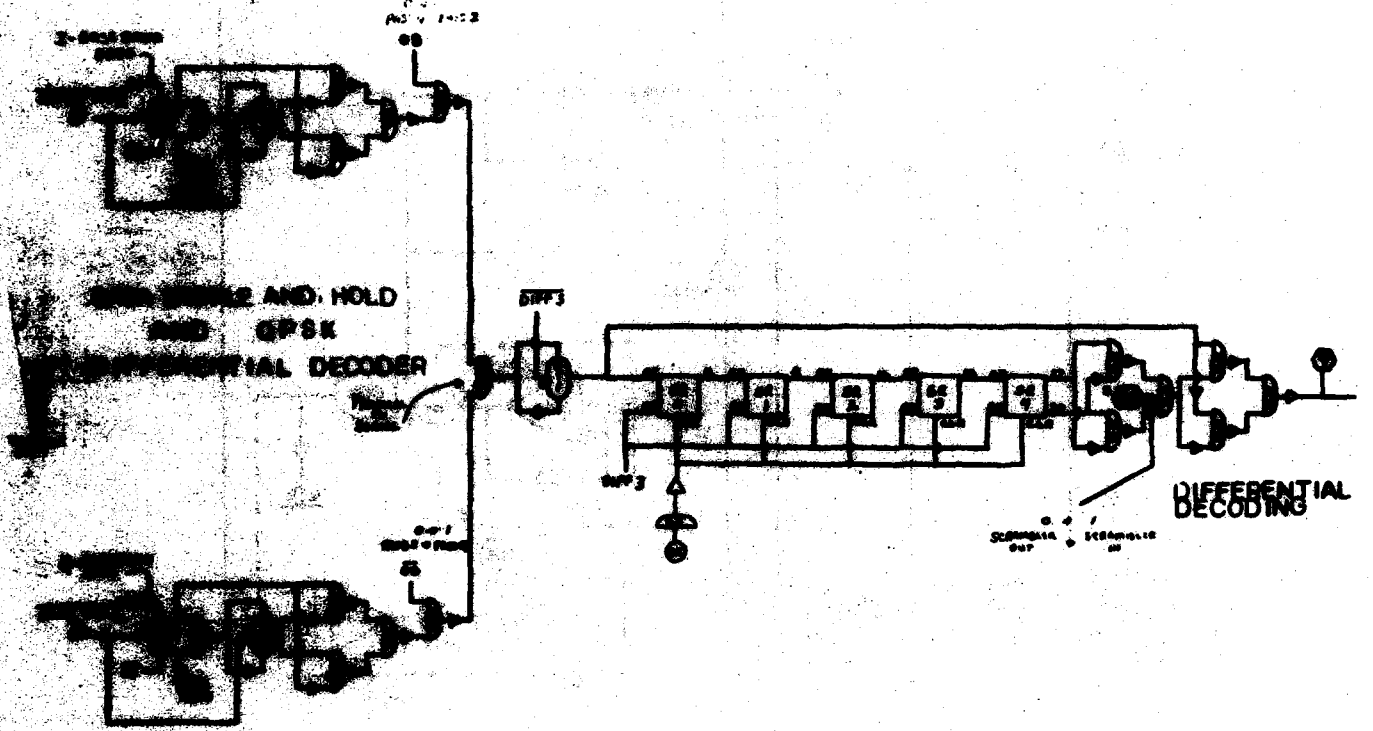
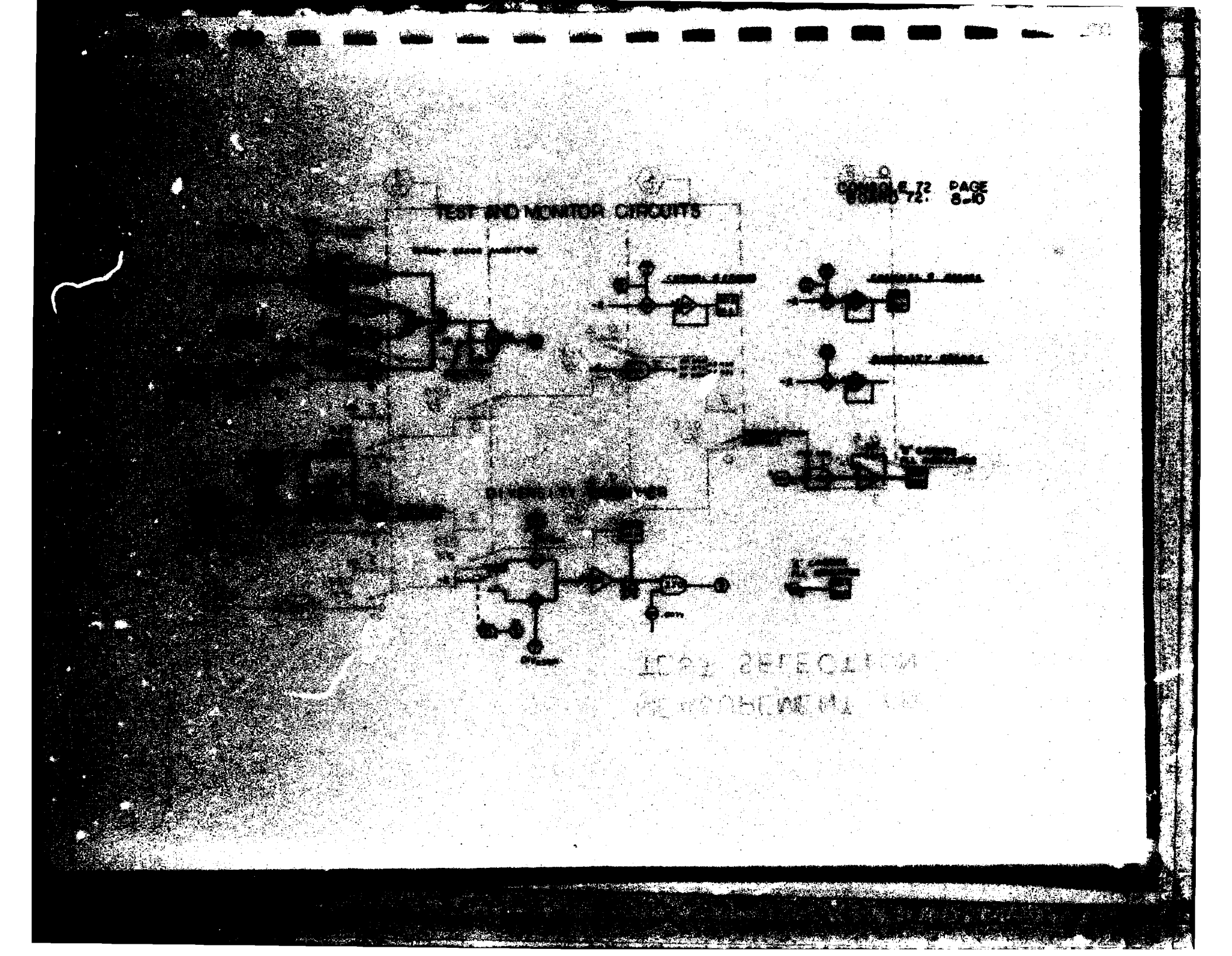
Q-RAIL

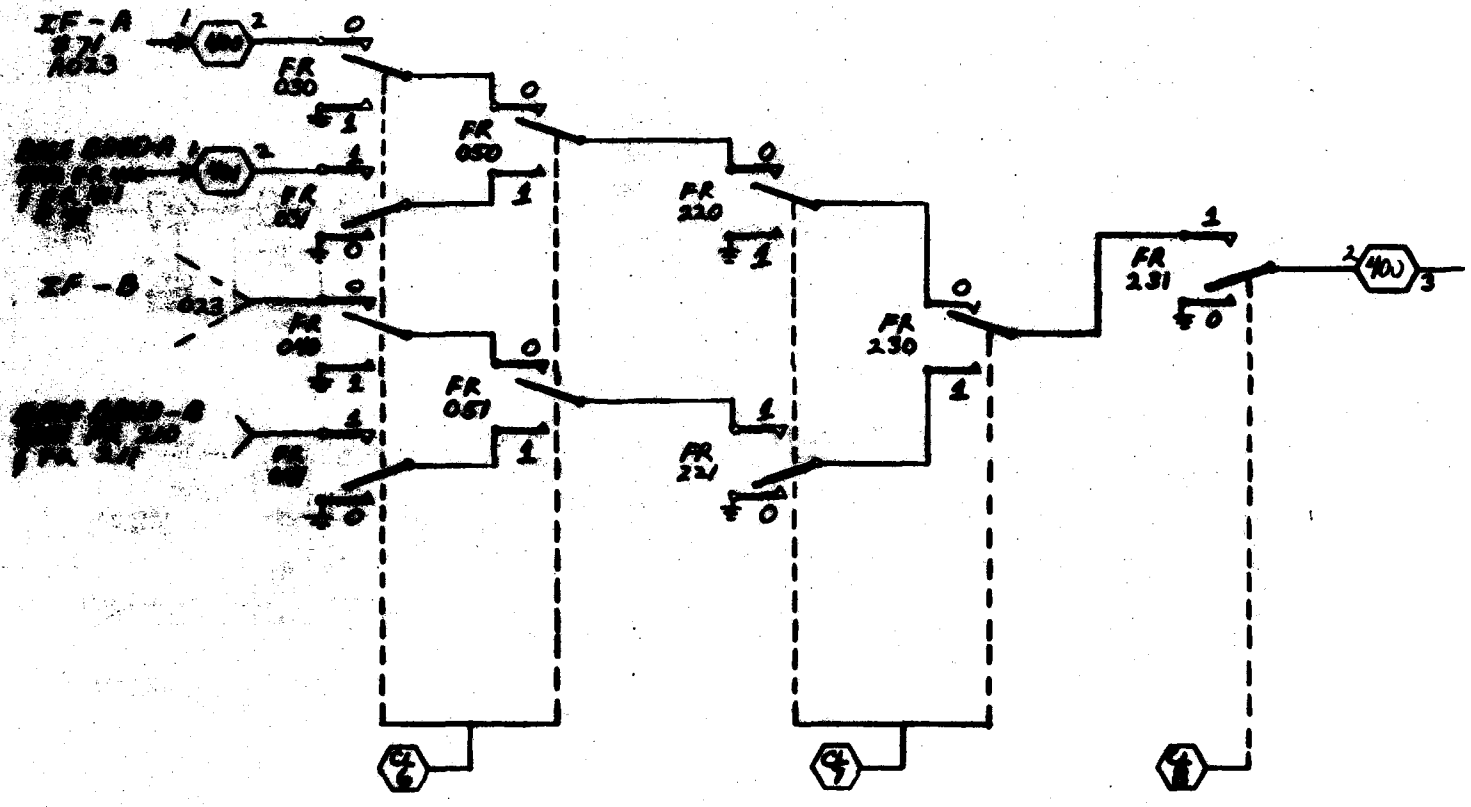


DATA REGENERATION

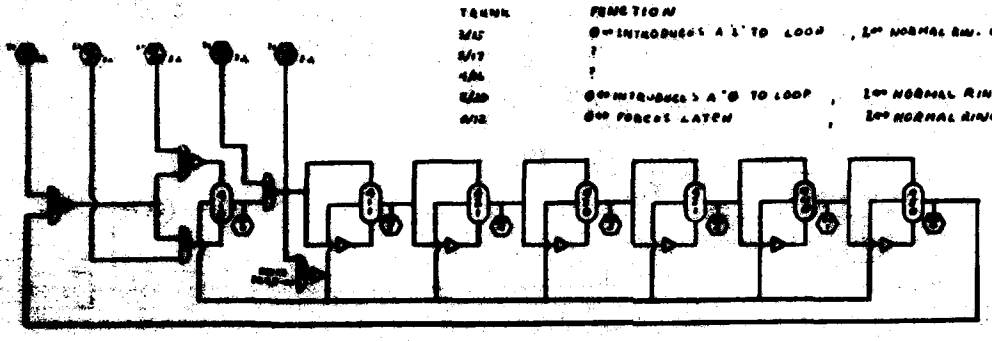



TEST AND MONITOR CIRCUITS

MEASUREMENT AND TEST SELECTION

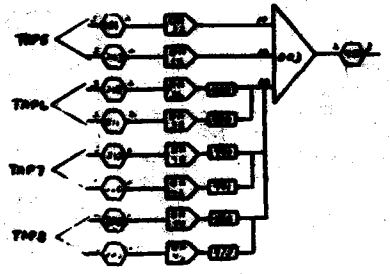


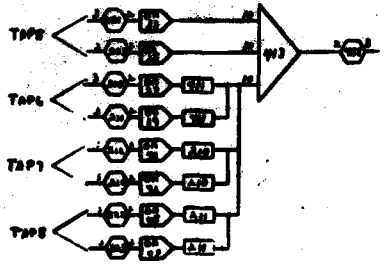
CONSOLE 72 RING COUNTER



TERM	FUNCTION
S/11	@ = INTRODUCES A '1' TO LOOP , 1 = NORMAL RING COUNTING OPERATION
S/12	?
S/13	?
S/20	@ = INTRODUCES A '0' TO LOOP , 1 = NORMAL RING COUNTING OPERATION
S/22	@ = FORCES LATCH , 1 = NORMAL RING COUNTING OPERATION

CHANNEL MEDIA MODEL





3-STAGE TRANSVERSAL FILTER

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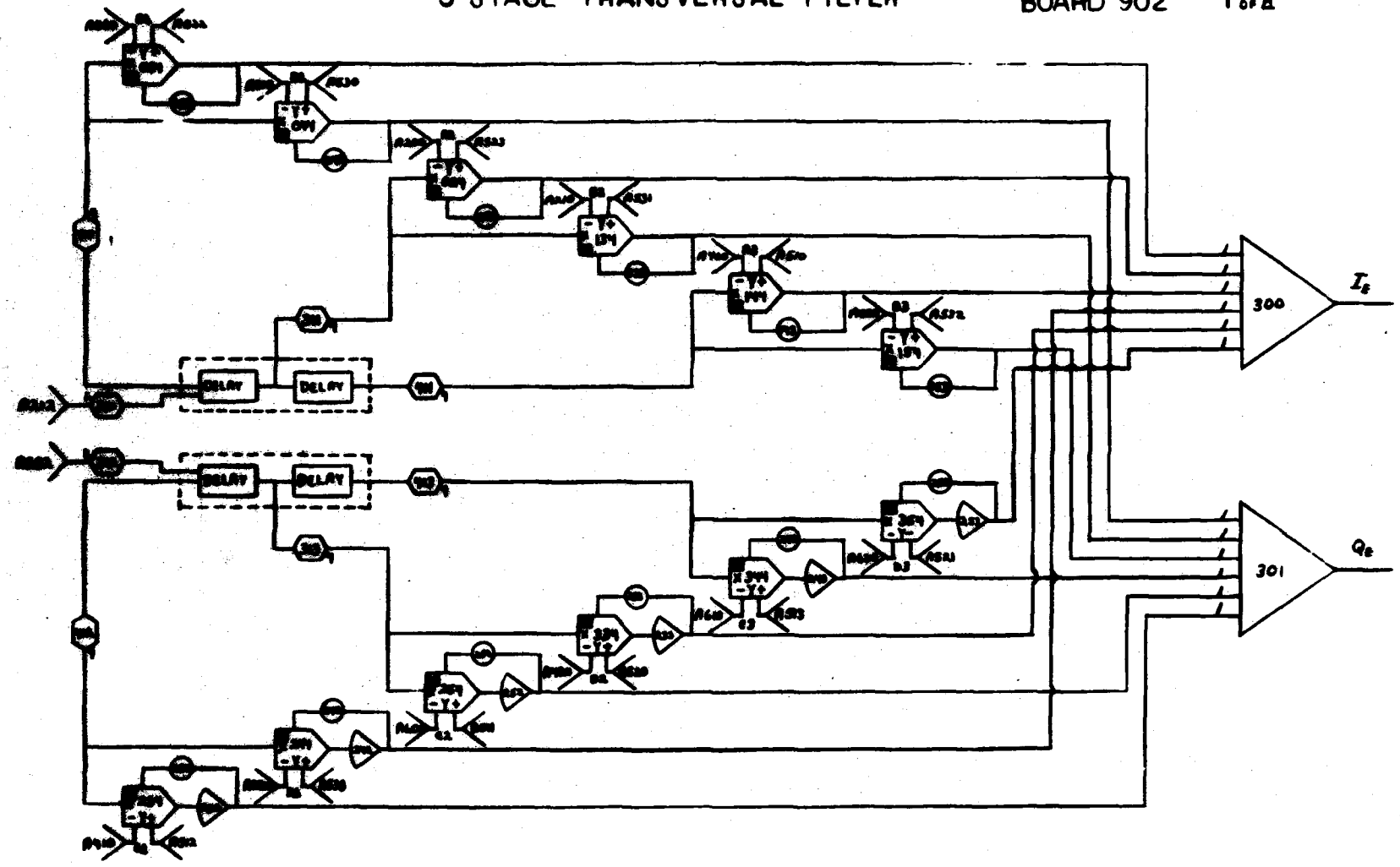

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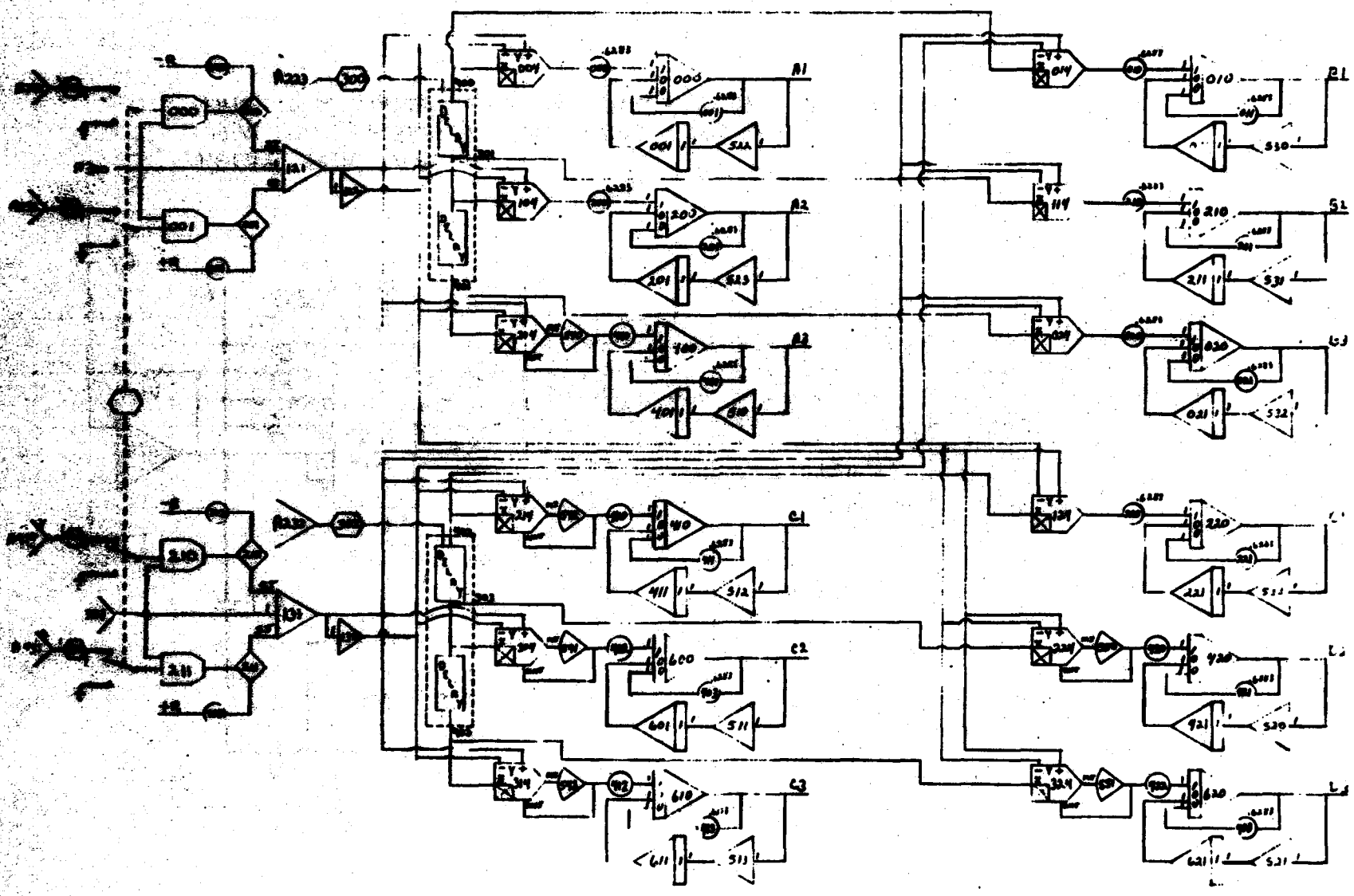

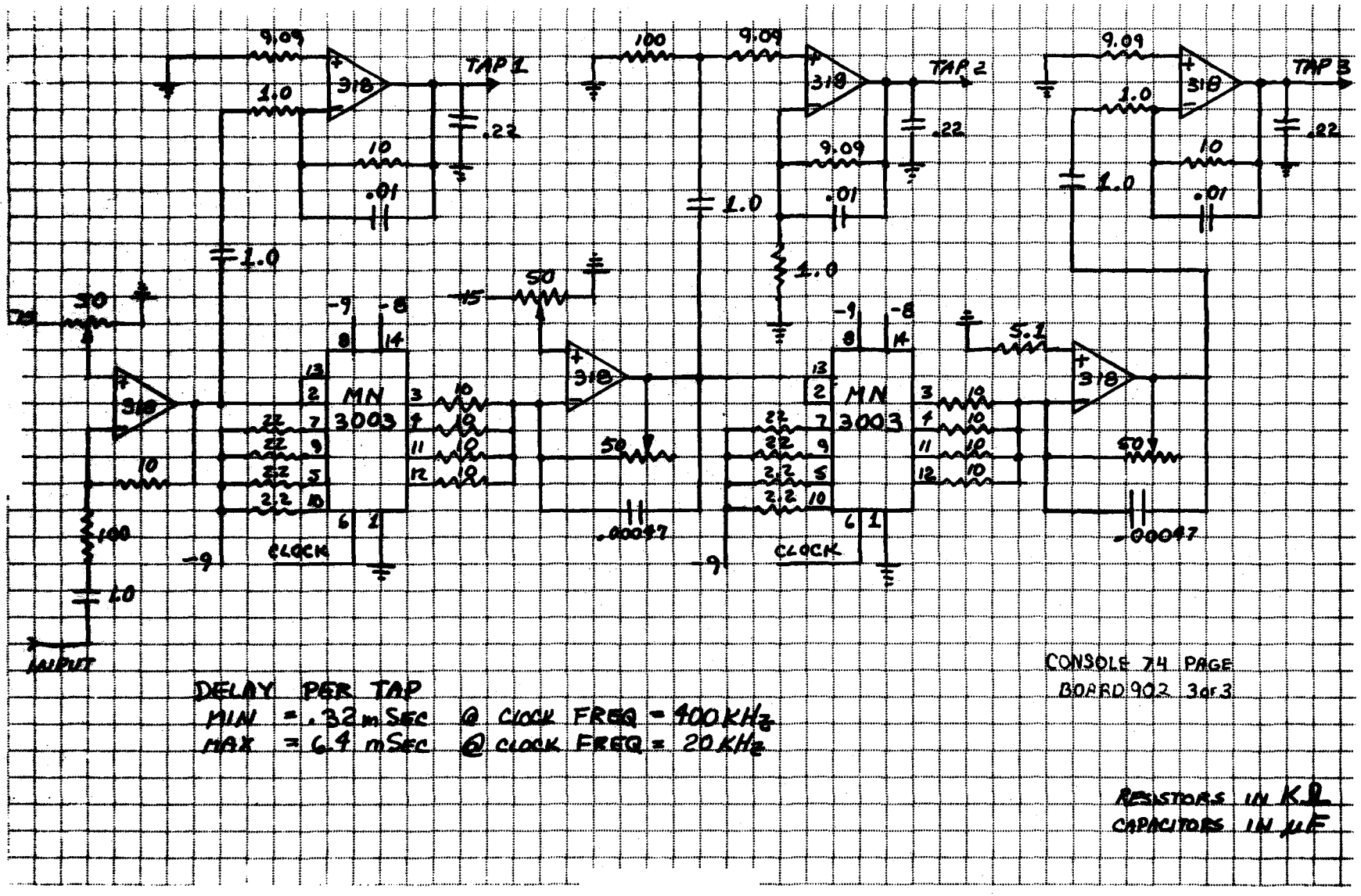

DELAY PER TAP
MIN = .32 mSec @ CLOCK FREQ = 400 KHz
MAX = 6.4 mSec @ CLOCK FREQ = 20 KHz

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RESISTORS IN KΩ
CAPACITORS IN μF